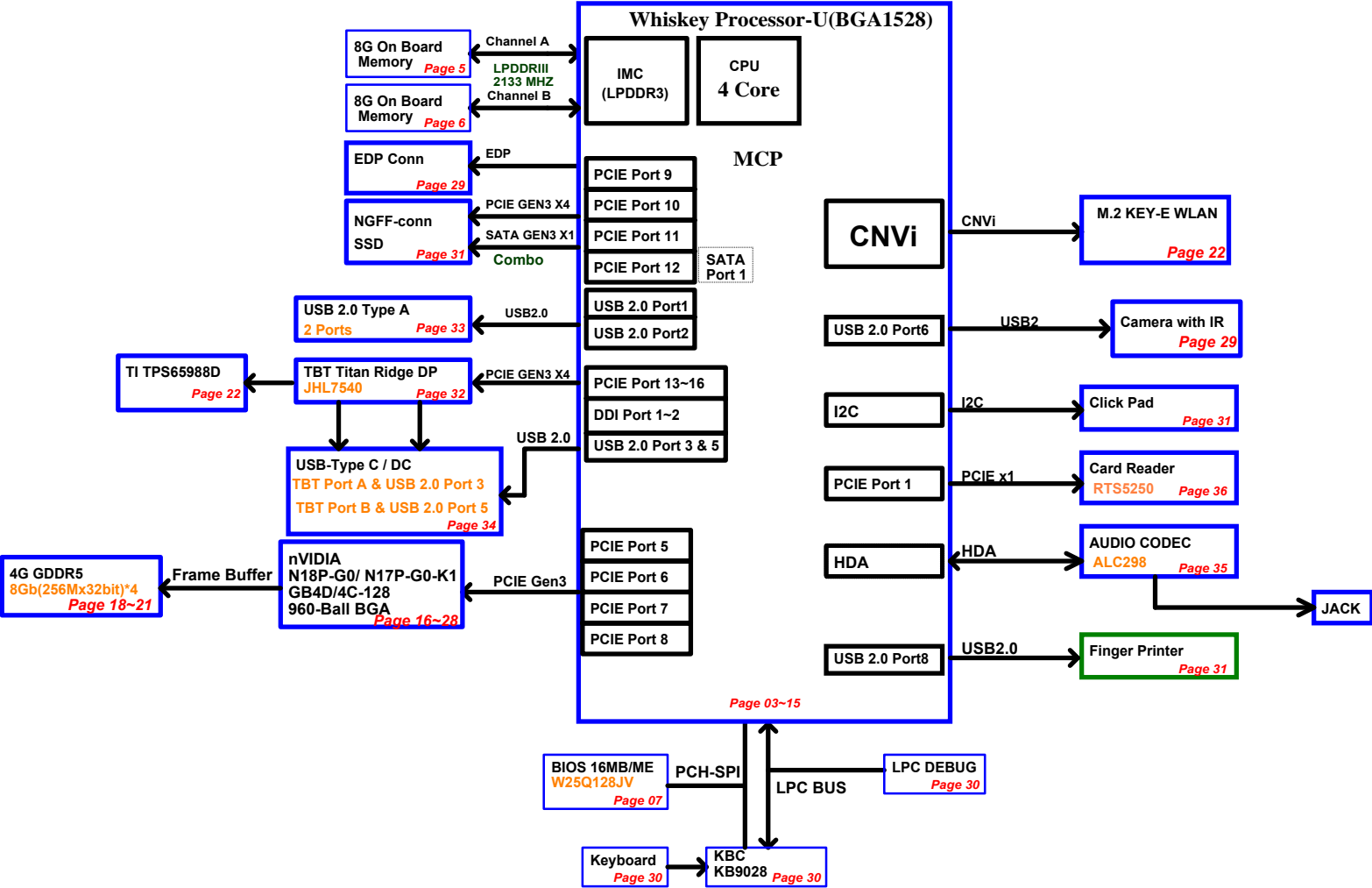


# Whiskey Lake Processor-U Platform MS-14C1 VER : A



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

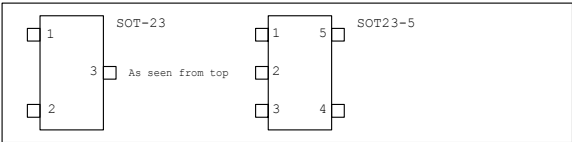
Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_05VSUS	1.0V power rail	+1_8VSUSPWROK
+1_8VSUS	1.8V power rail	3V5VPWROK
+1_2VDIMM/+1_8VDIMM	1.2V power rail DDR (off in S4-S5)	S4_DIMM_ON_AND
+VDDQ_CPU	1.2V power rail CPU DRAM (off in S4-S5)	S4_DIMM_ON_AND
+VCCST/+VCCPLL	1.0V power rail CPU (off in S4-S5)	+1_2VDIMM_PWRGD
+VCCSTG	1.0V power rail CPU (off in S3-S5)	RUND
+5VRUN	5.0V switched power rail (off in S3-S5)	RUND
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUND
+0_6VRUN	0.6V DDR Termination voltage (off in S3-S5)	DDR_VTT_CTRL
+1_8VRUN	1.8V power rail AUDIO (off in S3-S5)	RUND
+VCC_IO	1.0V rail for Processor & PCH (off in S3-S5)	RUND
+VCC_SA	0.55V to 1.15V Voltage for Processor	VR_ON
+VCC_GT	0.55V to 1.52V Core Voltage for Processor	VR_ON
+VCC_CORE	0.55V to 1.5V Voltage for Processor	VR_ON

Net Naming Conventions

Suffix
# = Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

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PCB Footprints



POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+3VSUS	+*VSUS	+*VRUN	+VTT_CORE	Clocks
S0( Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON
S3( Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	ON	OFF	OFF	OFF
S4( Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF	OFF
S3( Suspend to RAM) WOL_EN	LOW	HIGH	HIGH	ON	ON	ON	OFF	OFF	OFF
S4( Suspend to Disk) WOL_EN	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF	OFF
S5 (Soft OFF) WOL_EN	LOW	LOW	LOW	ON	ON	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V\*SUS will always keep high

MICRO-STAR INT'L CO.,LTD.

Title

PLATFORM

Size

Custom

Document Number

MS-14C1

Date:

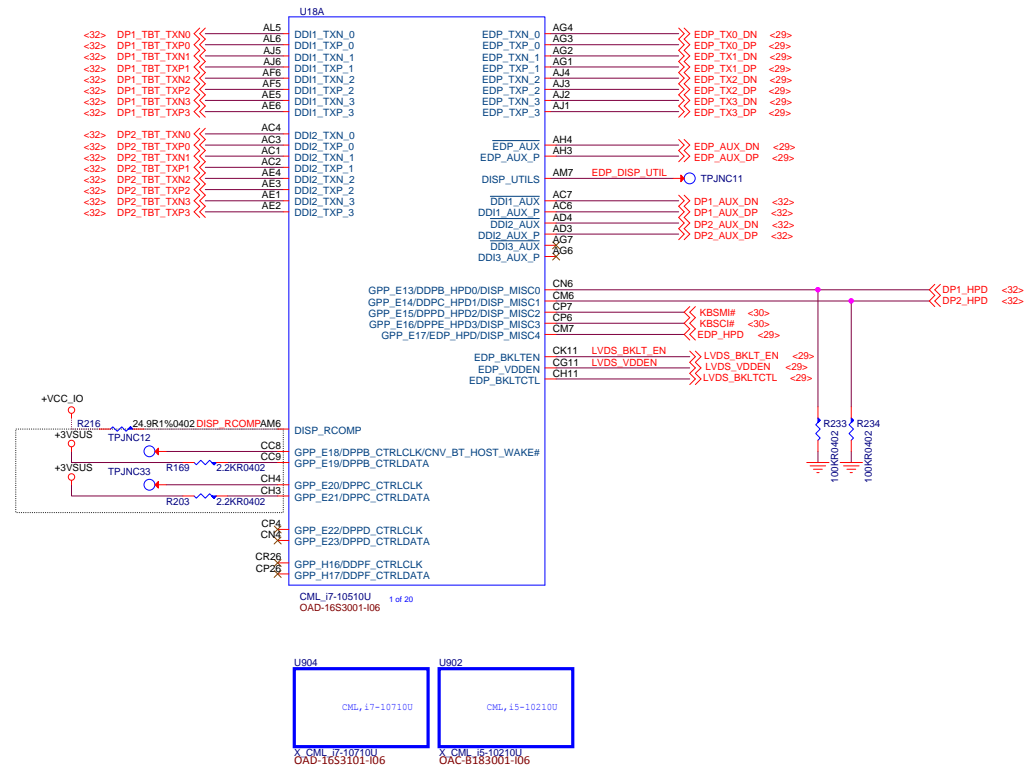
Wednesday, July 17, 2019

Sheet

2 of 56

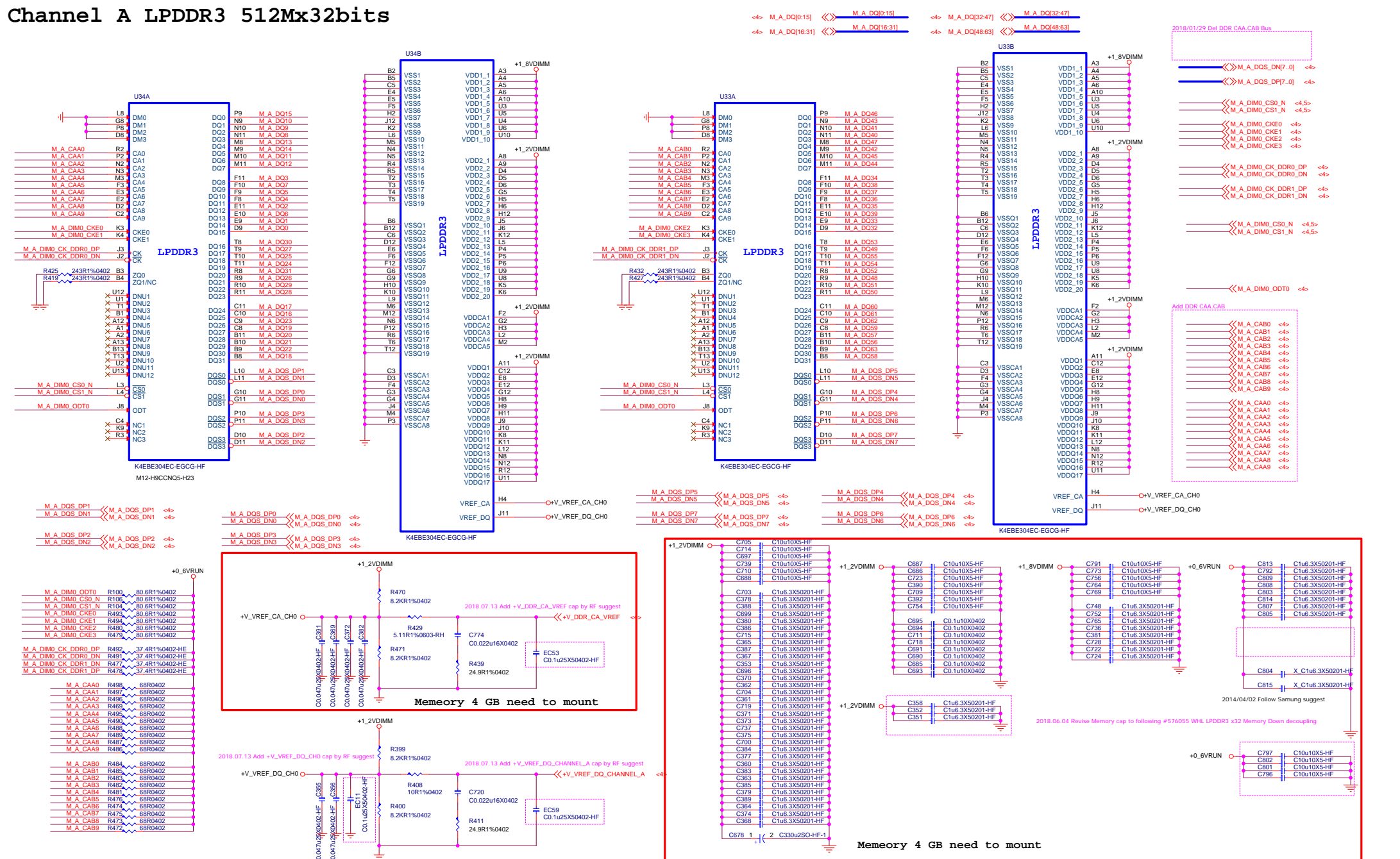
Rev

0A

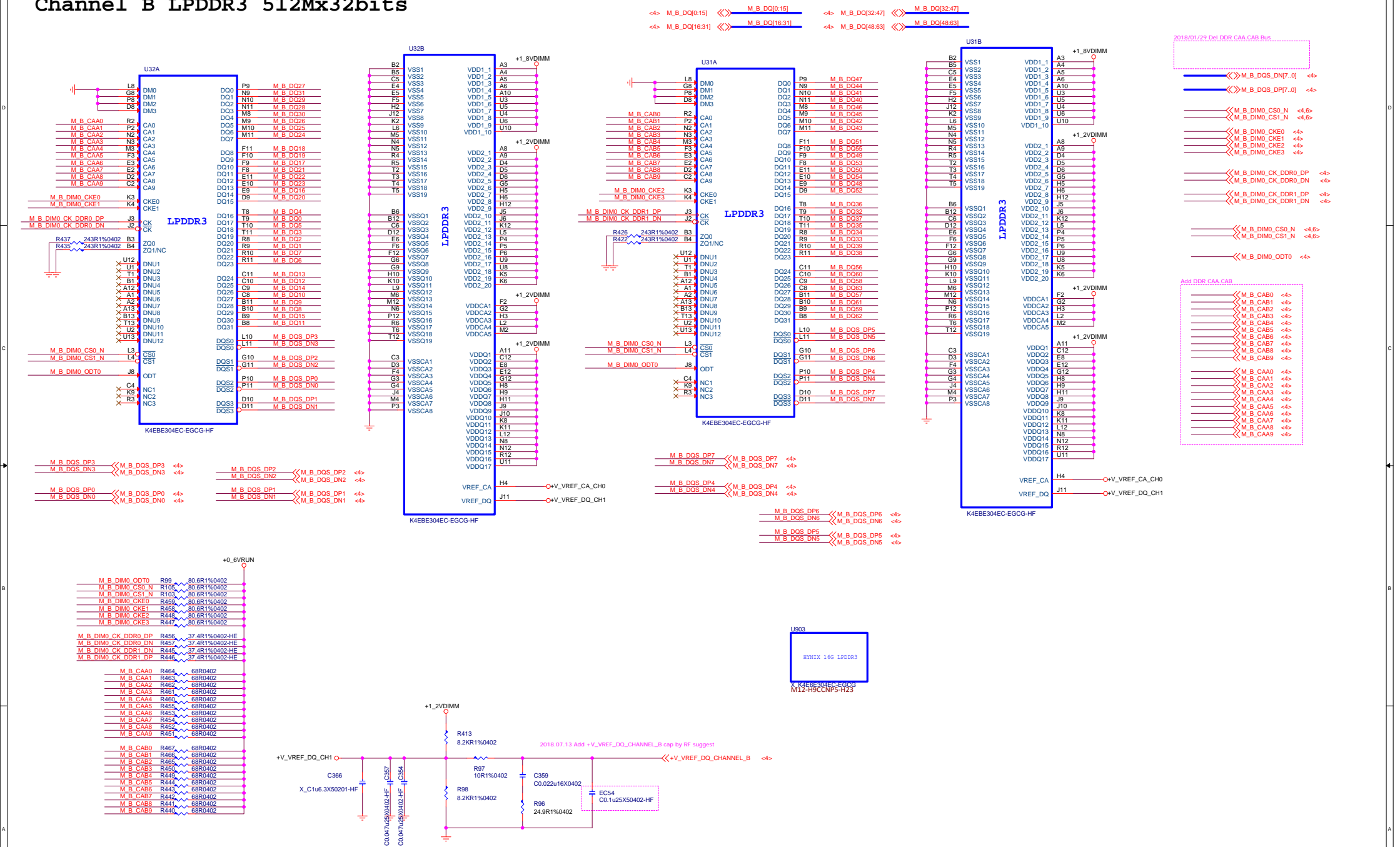




Channel A LPDDR3 512Mx32bits



**Channel B LPDDR3 512Mx32bits**





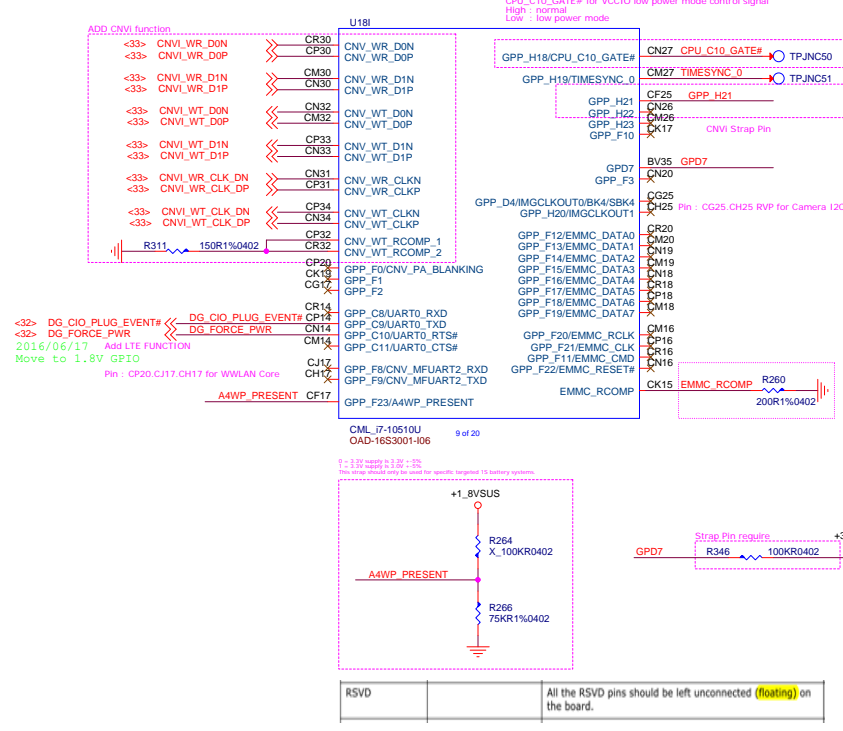
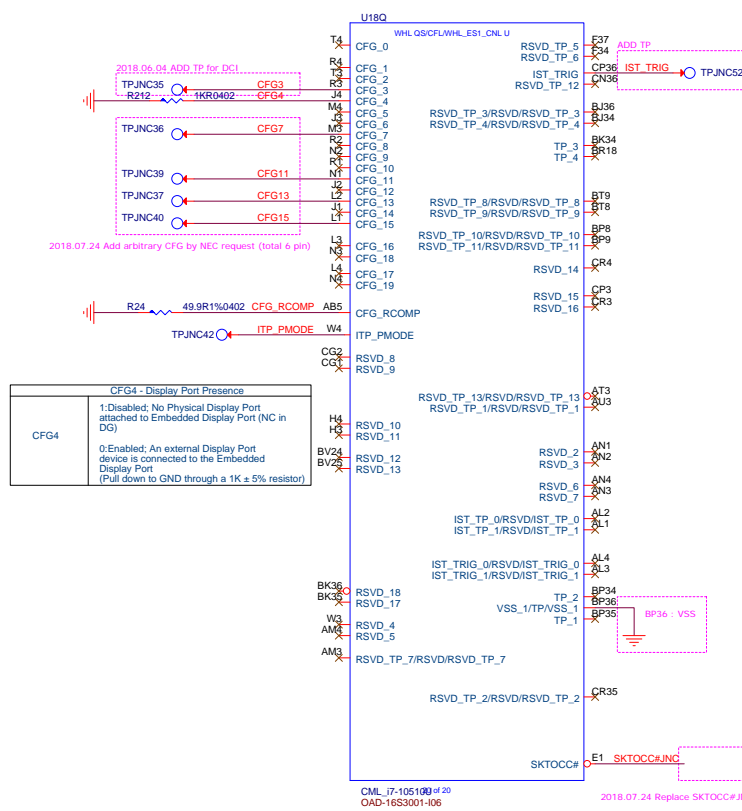


2018.06.01 Revise memory configuration table

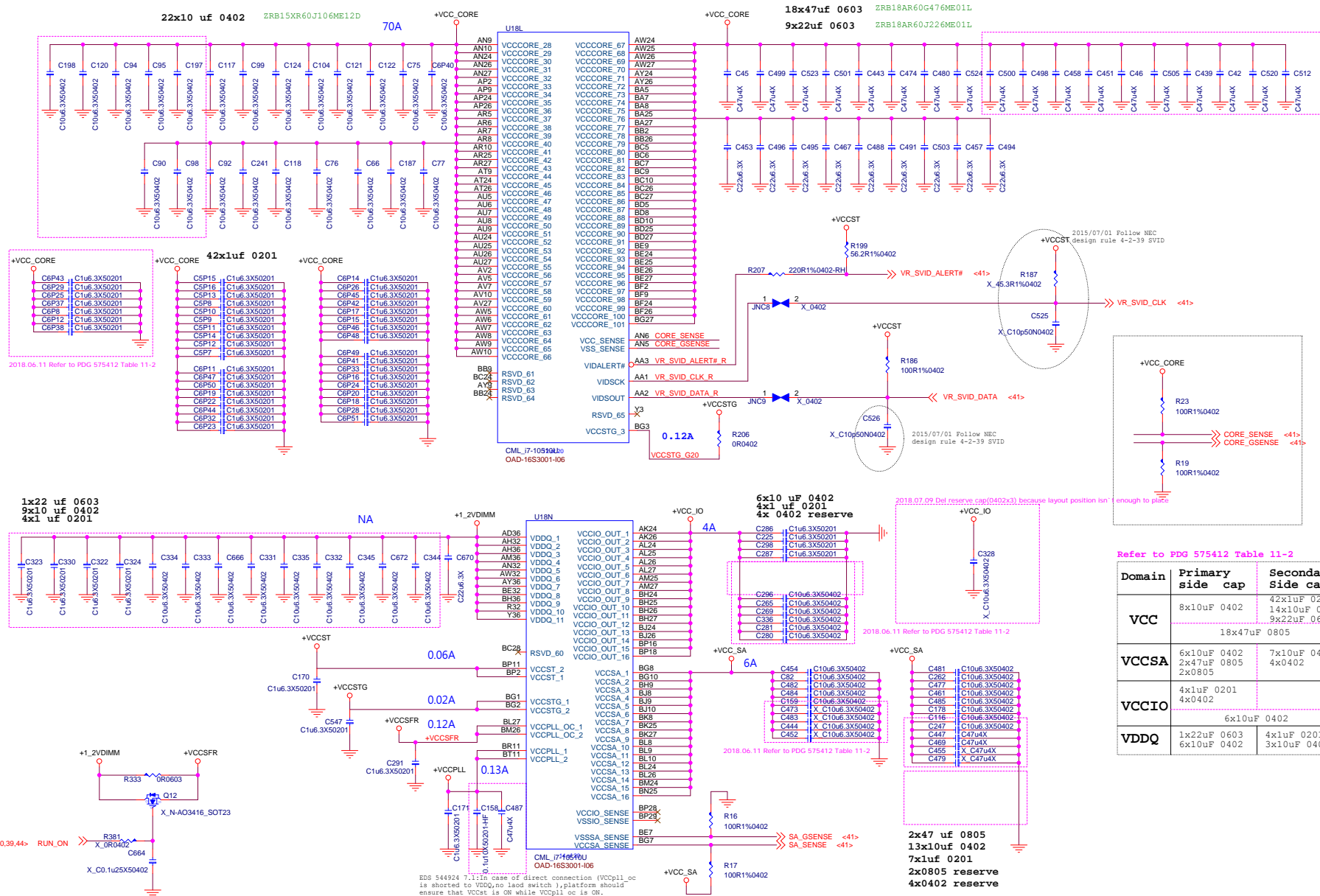


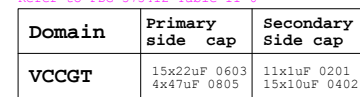


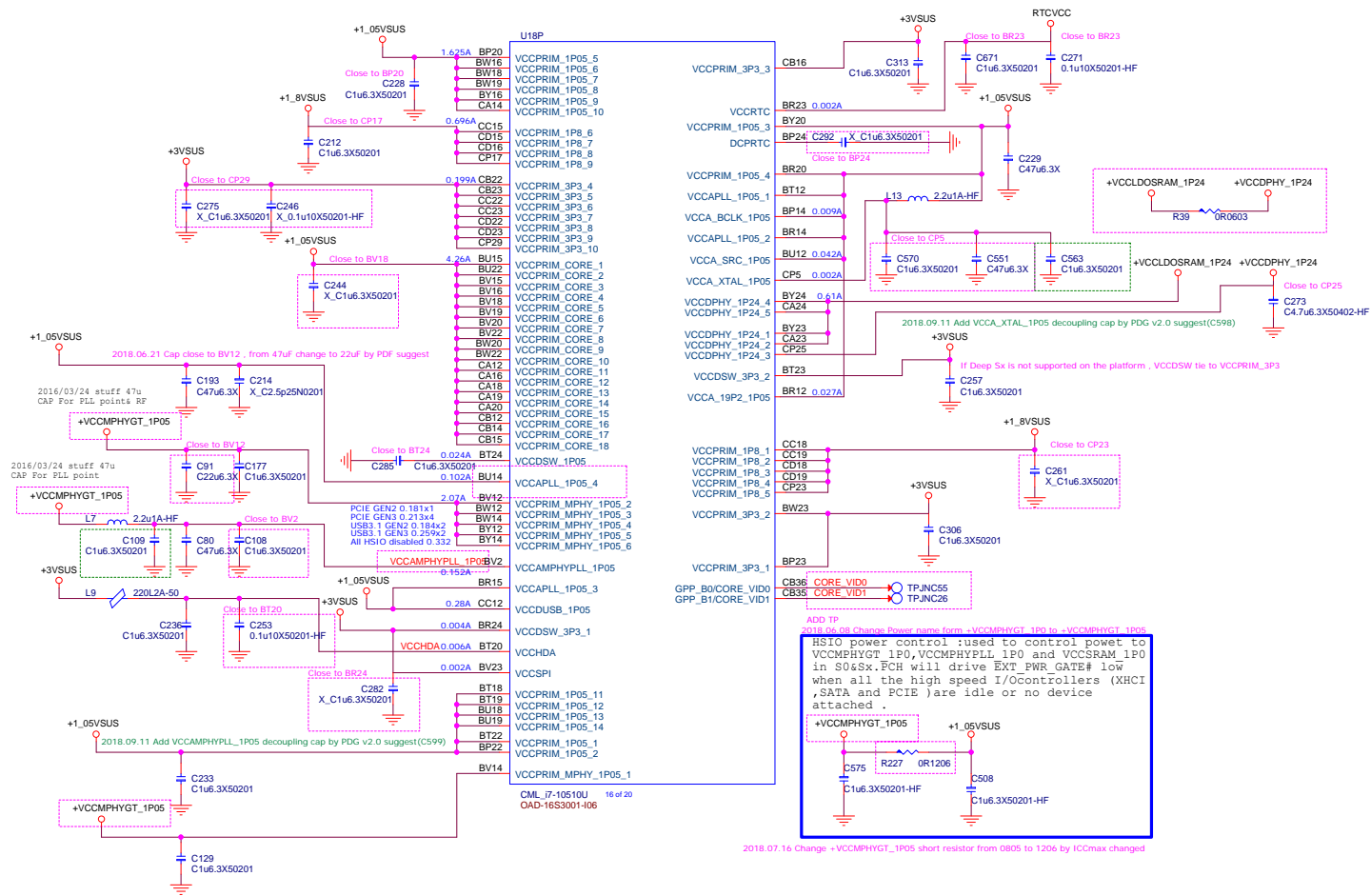




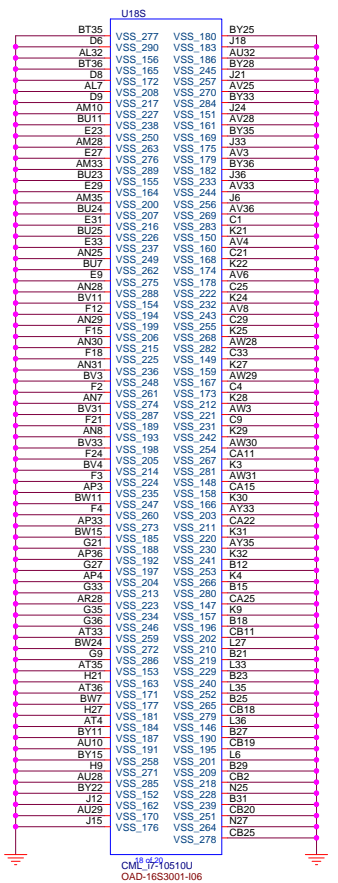
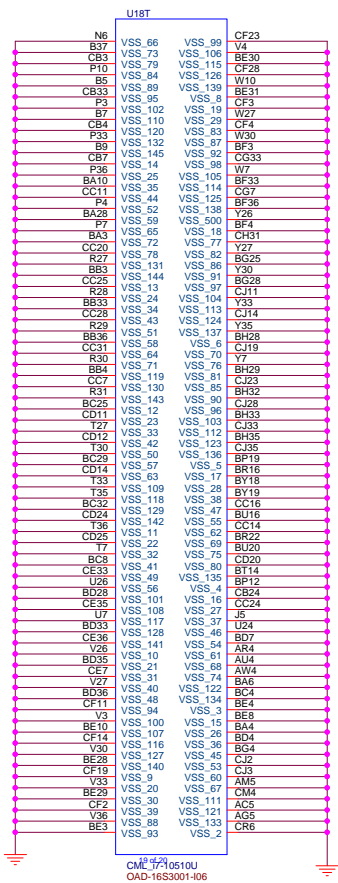
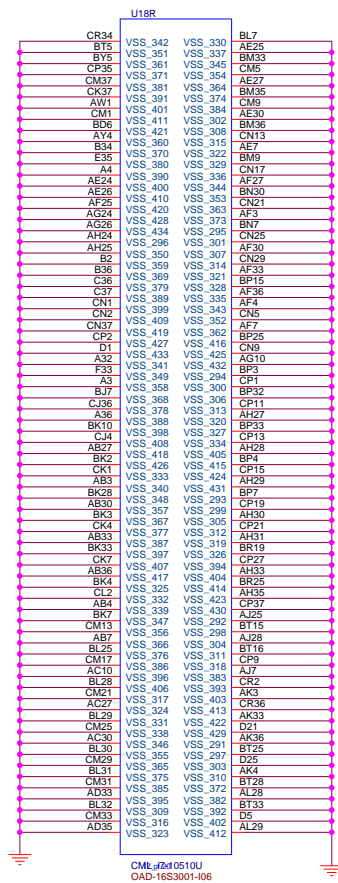
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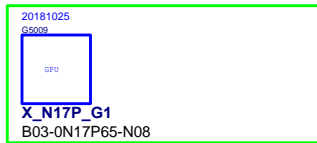






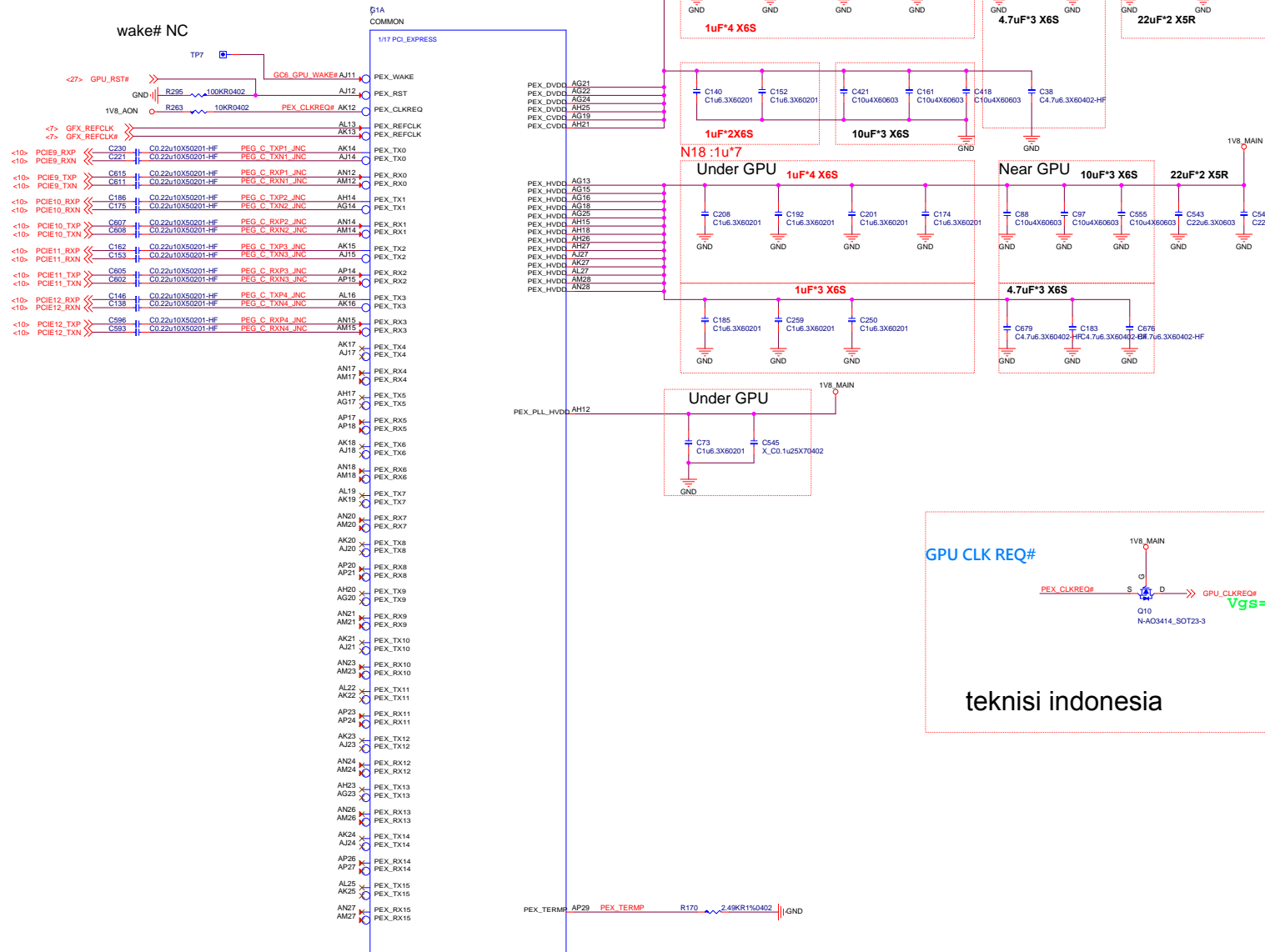


## GPU PCI EXPRESS



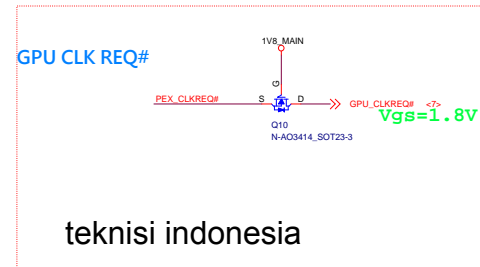
N18:0.47u\*15,change 10,4.7u\*3,10u\*3,22u\*2  
N17:1u\*4,4.7u\*2,10u,22u\*1

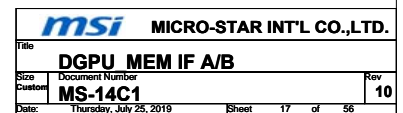
N18 :1u\*6



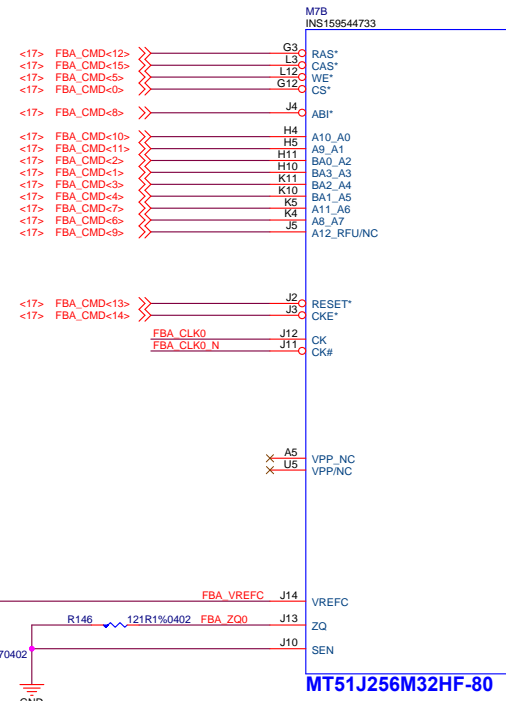
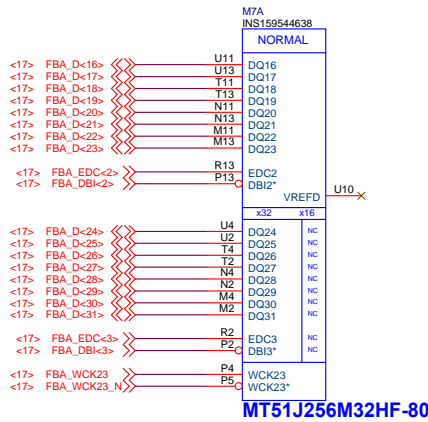
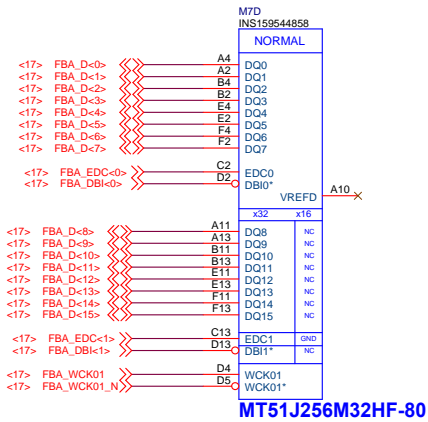
PEX_DVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5R
N17P	4	2	1	1
N18P	6	3	3	2

3X0603	PEX_HVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5R
	N17P	4	2	2	1
	N18P	7	3	3	2

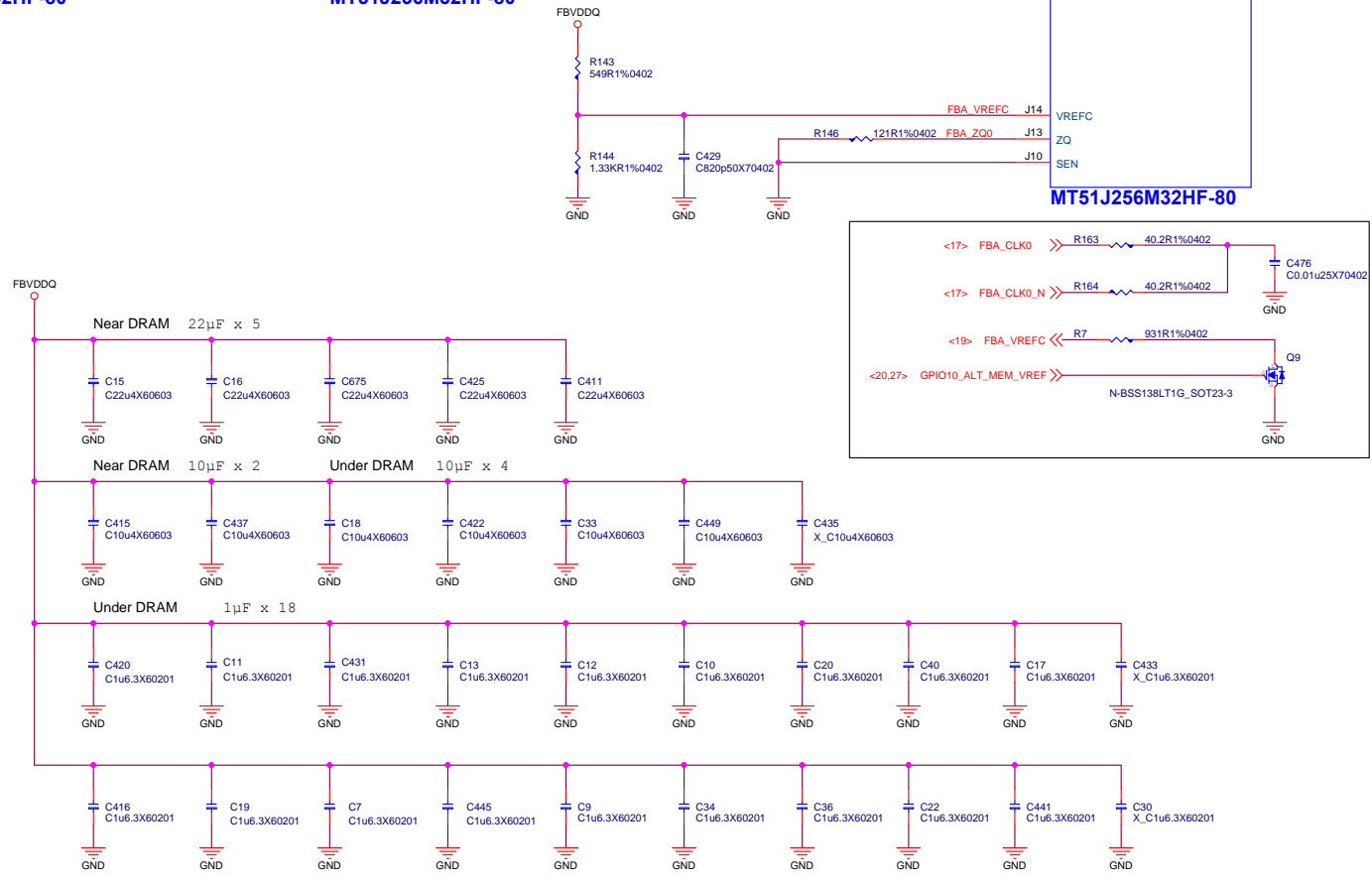
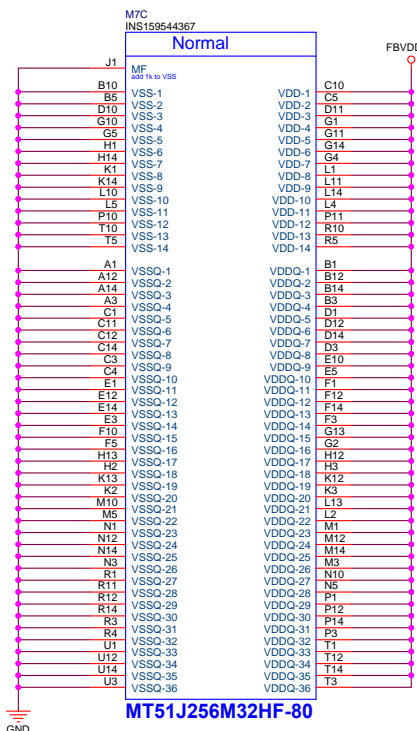




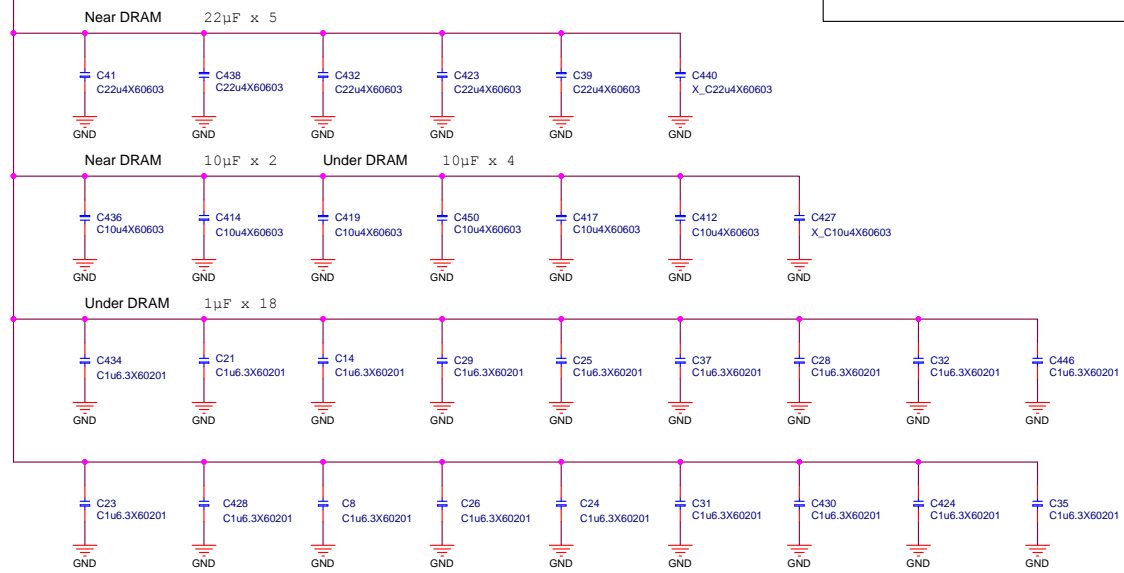
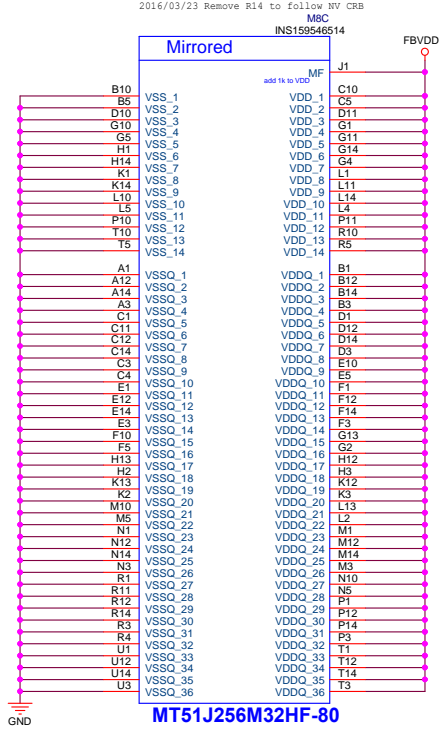
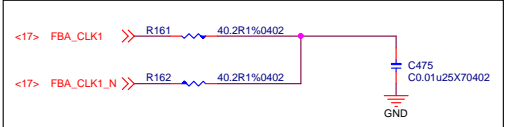
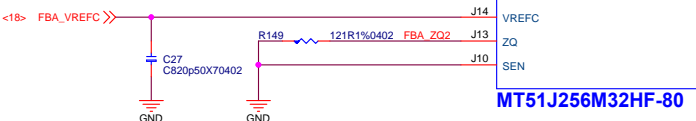
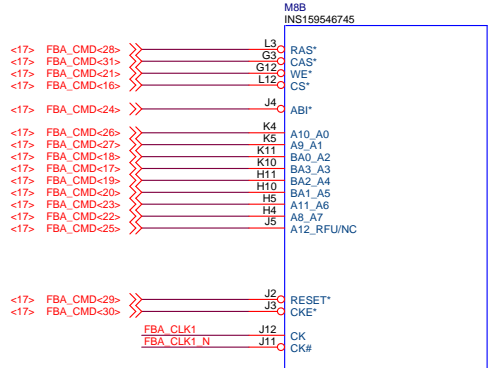
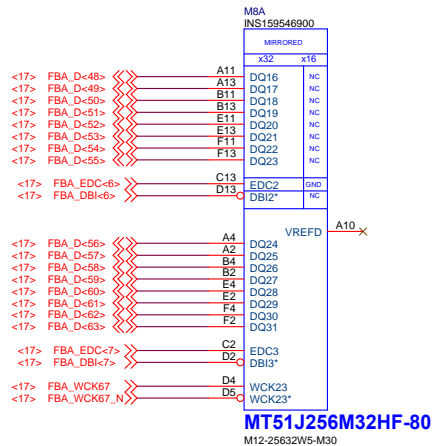
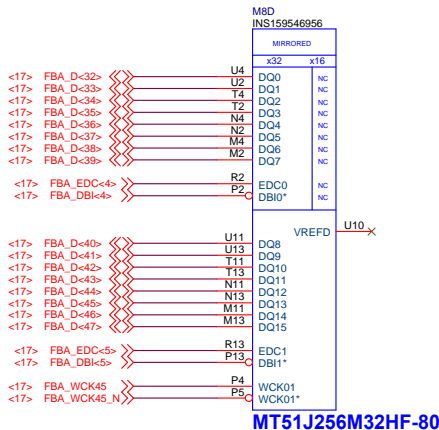
# DGPU\_GDDR5 FrameBuffer A0



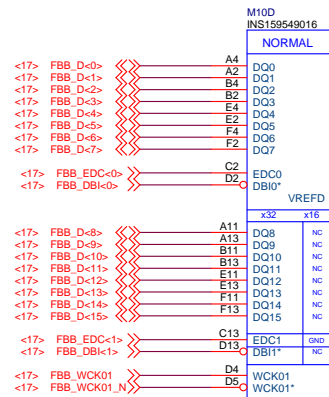
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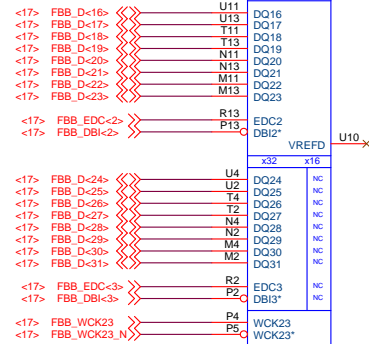
DGPU\_GDDR5 FrameBuffer A1



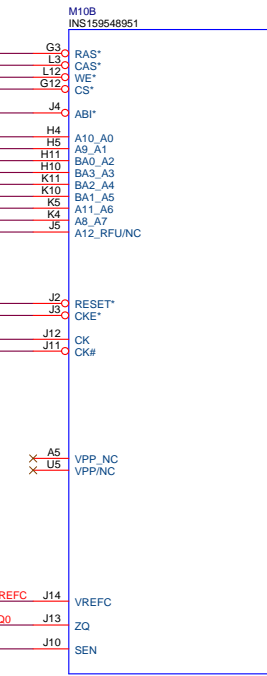
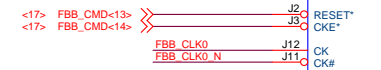
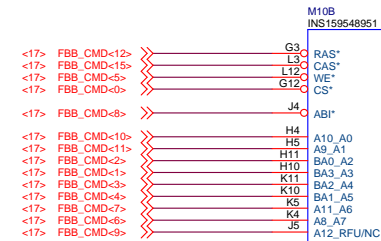
## DGPU\_GDDR5 FrameBuffer B0



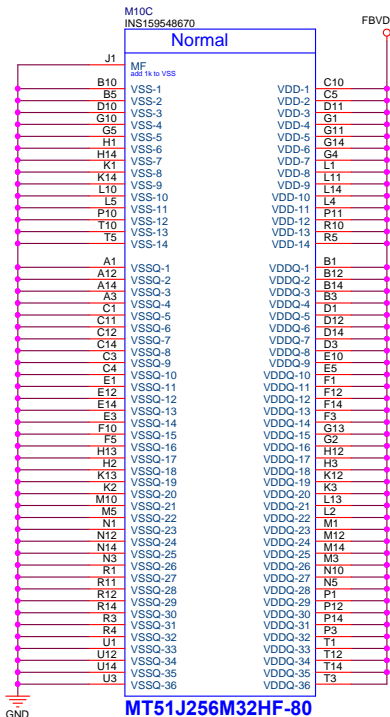
MT51J256M32HF-80



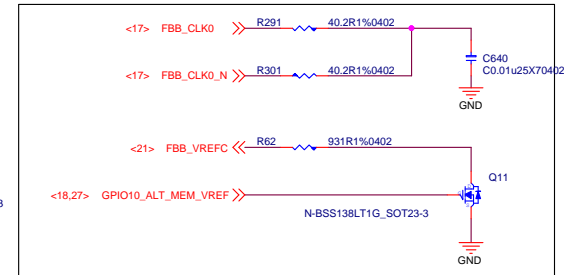
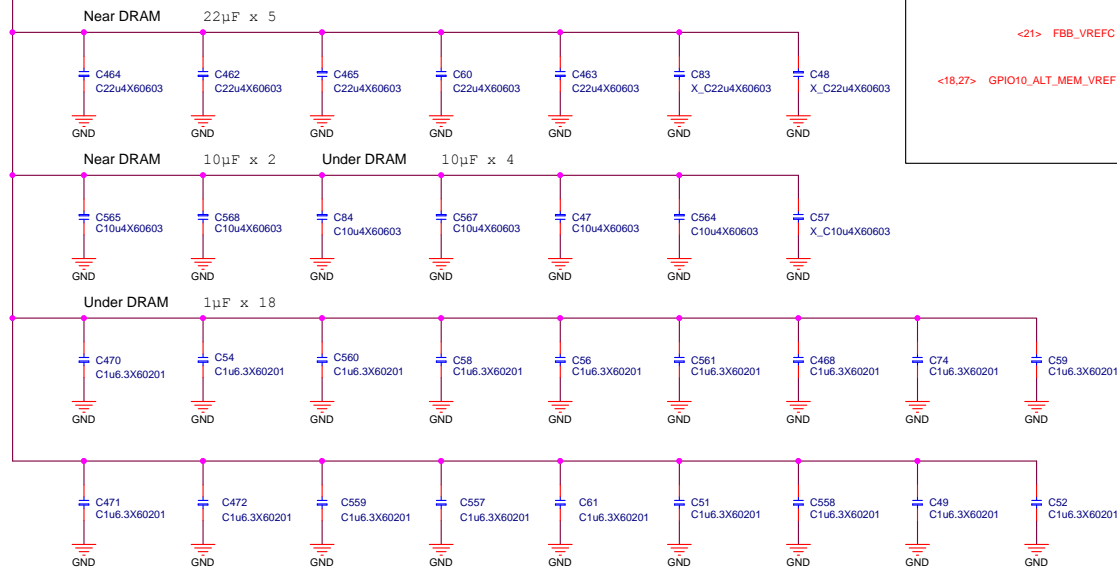
MT51J256M32HF-80



MT51J256M32HF-80

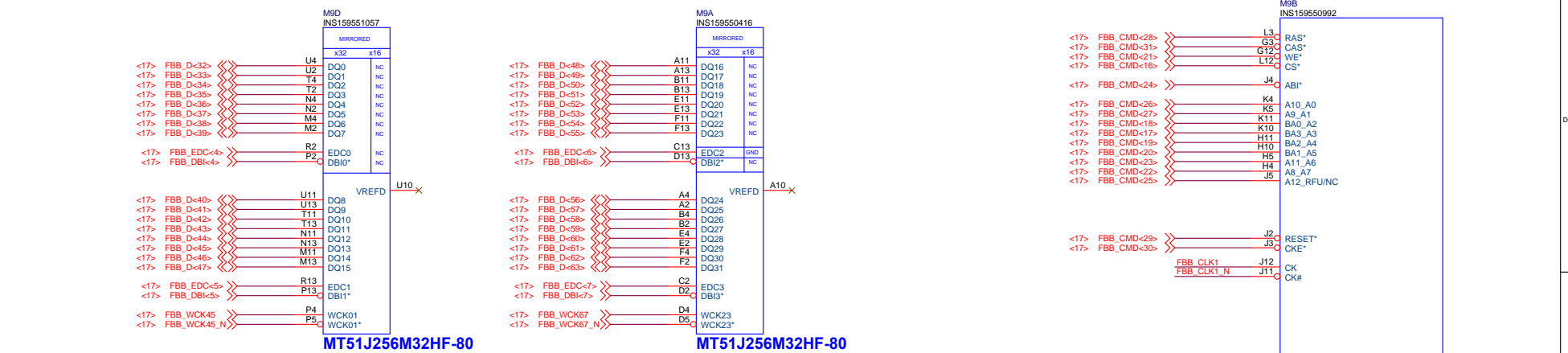


MT51J256M32HF-80

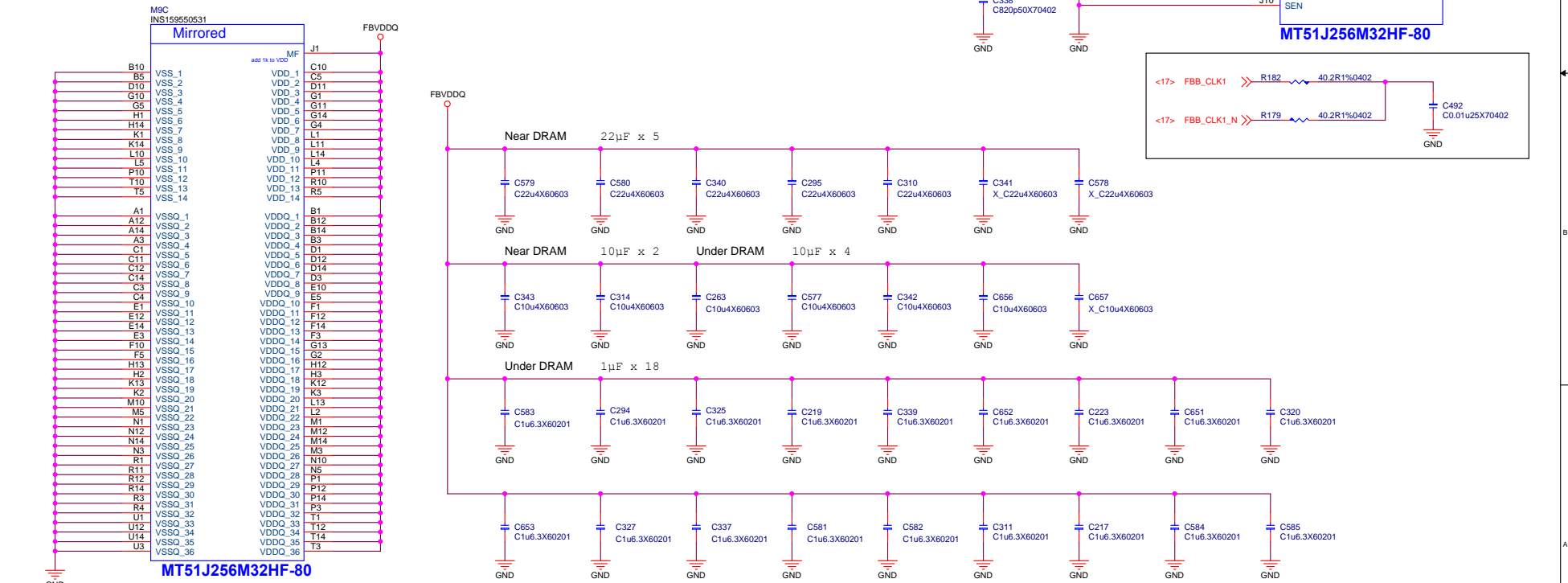




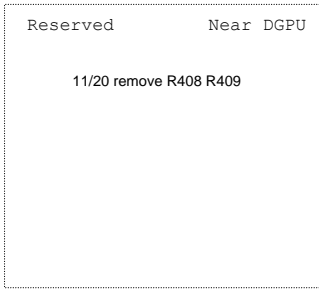
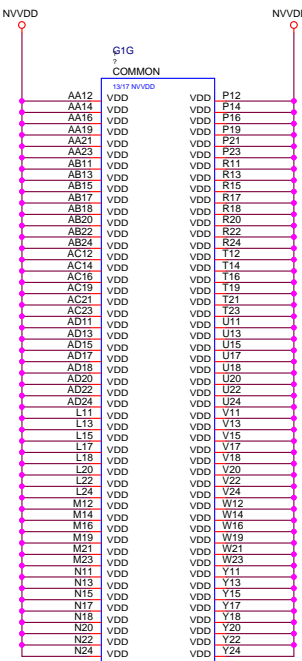
DGPU\_GDDR5 FrameBuffer B1



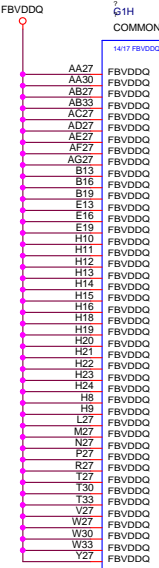
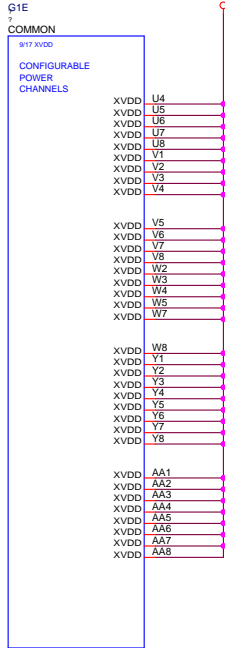
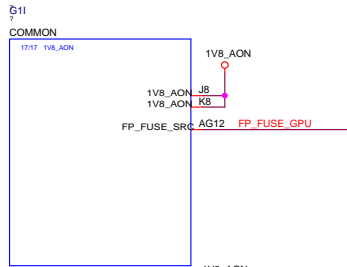
Vinafix.com



# GPU NVVDD, FBVDDQ



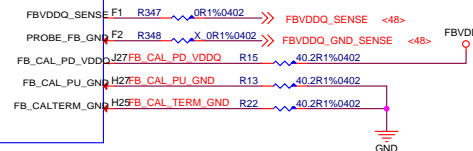
1V8_AON	0.1uF X7R	1uF X6S	4.7uF X6S
N17P	2	1	1
N18P	0	5	3



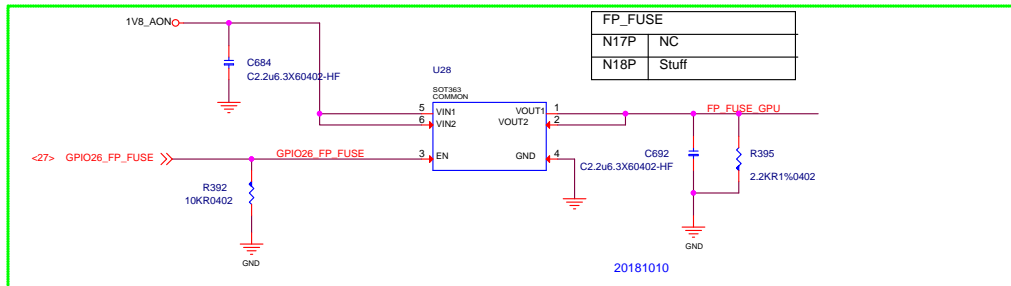
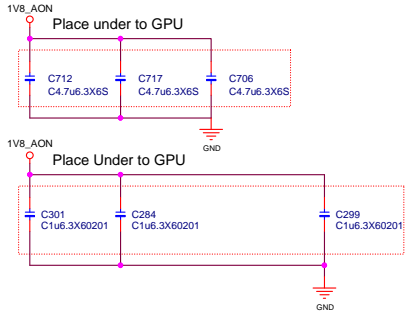
N17P 60.4 OHM  
N18P 40.2 OHM

FBCALTERM1  
R11-604AT12-W08  
X\_60.4R1%0402

FBCALTERM2  
R11-402AT12-W08  
X\_40.2R1%0402

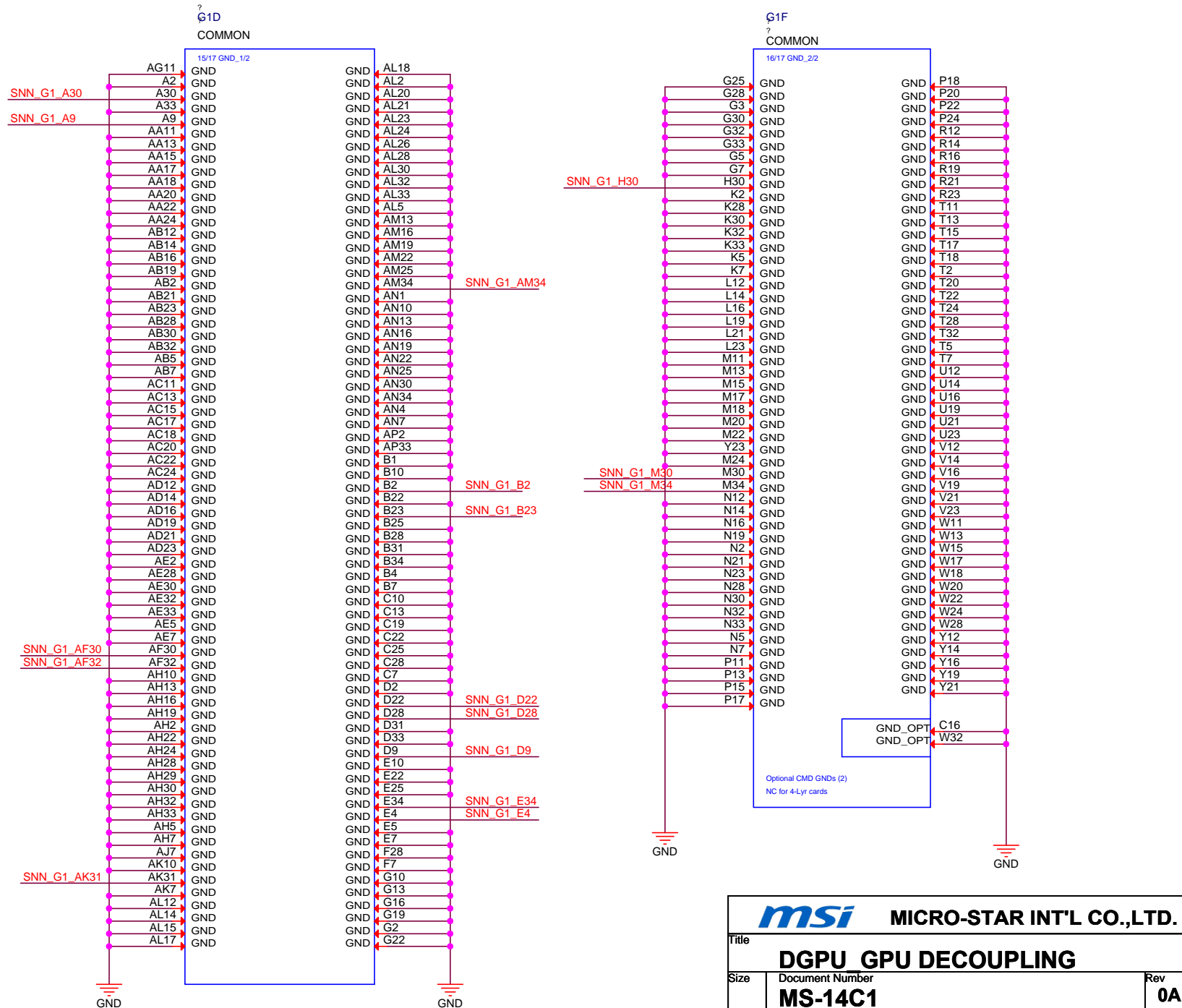


FB_CALTERM	
N17P	FB_CALTERM_GND 60.4OHM
N18P	FB_CALTERM_GND 40.2ohm



# DGPU GND

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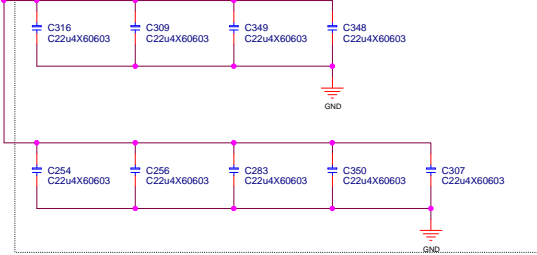
<b>msi</b> MICRO-STAR INT'L CO.,LTD.	
Title <b>DGPU GPU DECOUPLING</b>	
Size	Document Number <b>MS-14C1</b>
Date: Thursday, July 25, 2019	Sheet 23 of 56
Rev <b>0A</b>	

## NVVD

N18P  
330uF x0  
4.7uF x0  
22uF x15  
10uF x 0+34(Under GPU34,Near GPU0)  
0.47uF x26  
1uF x0

N17P  
330uF x1  
4.7uF x2  
22uF x10  
10uF x 11+21(Under GPU21,Near GPU11)  
0.47uF x0  
1uF x13

Place Near to GPU 22uF\*15pcs

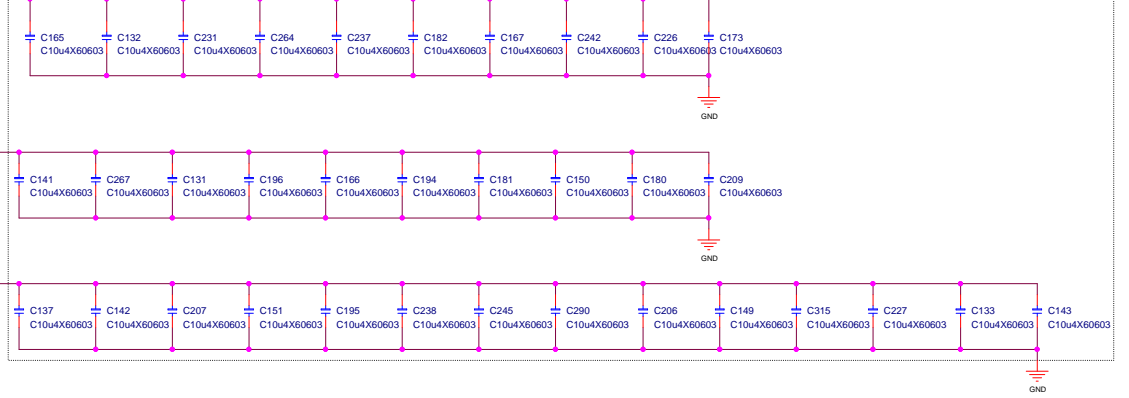


NVVD	1uF X7R	4.7uF X6S	10uF X6S	22uF X6S
N17P	13	2	31	10
N18P	13	0	34	15

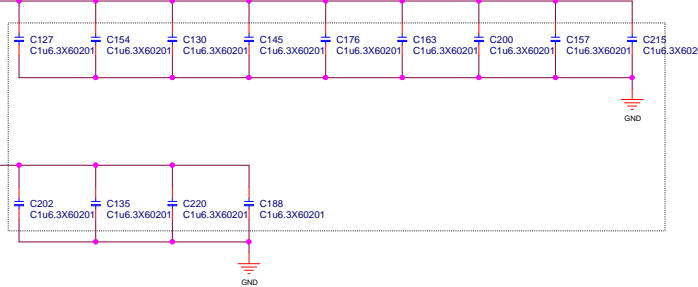
## GPU DECOUPLING

NVVD

Place Under to GPU 10uF\*34pcs



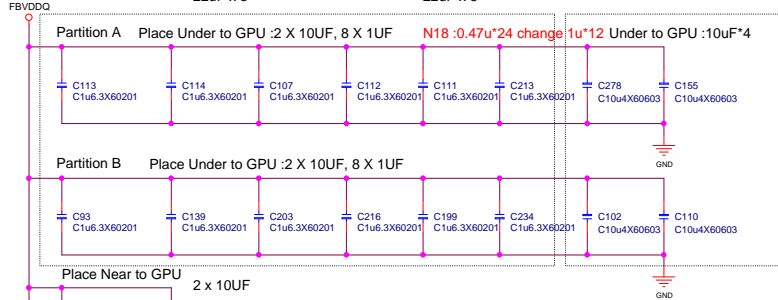
Place under to GPU 18pcs 1u instead of 0.47u N18 :0.47u\*26 change 1u\*13



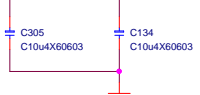
## FBVDDQ

1uF x 16 N18P  
10uF x 6  
22uF x 5

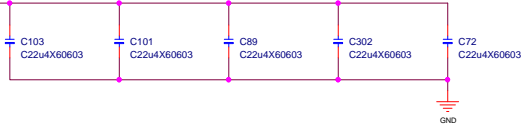
1uF x 12 N17P  
10uF x 6  
22uF x 5



Place Near to GPU 2 x 10UF

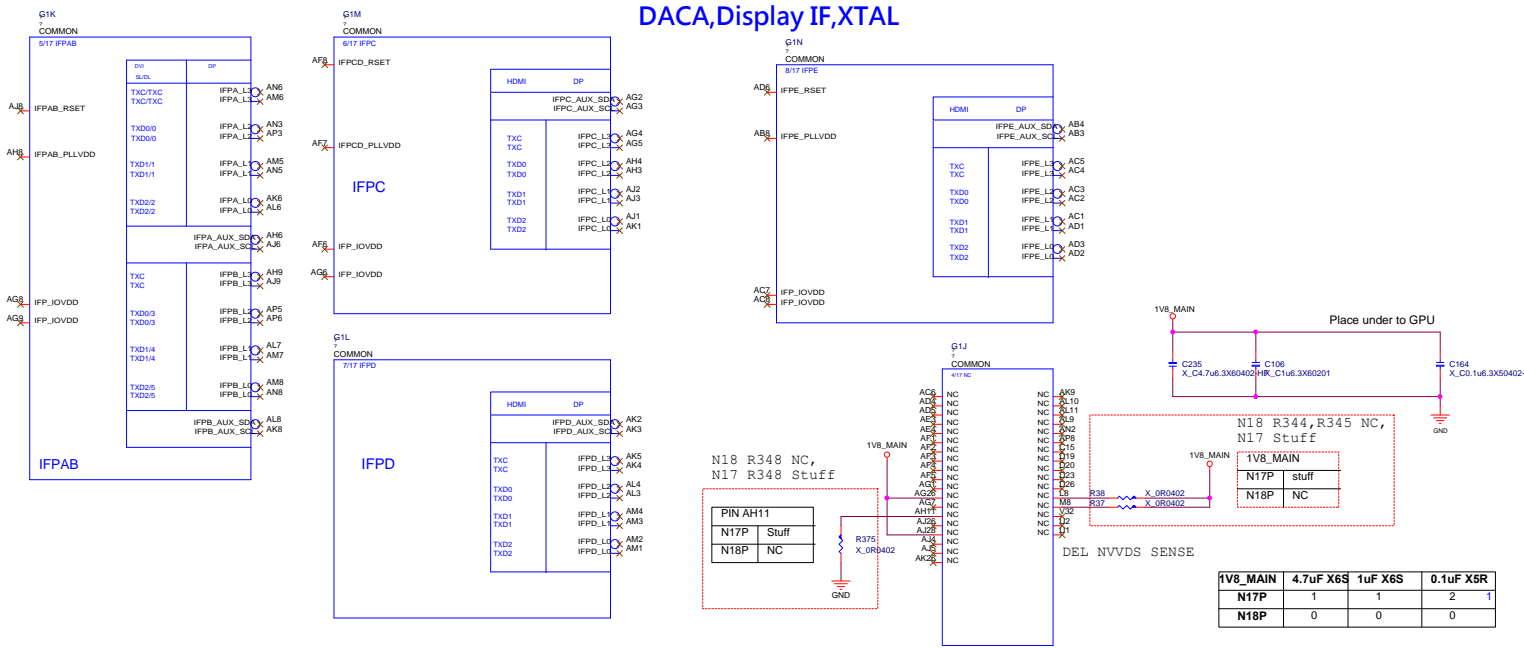


Place Near to GPU 5 x 22UF

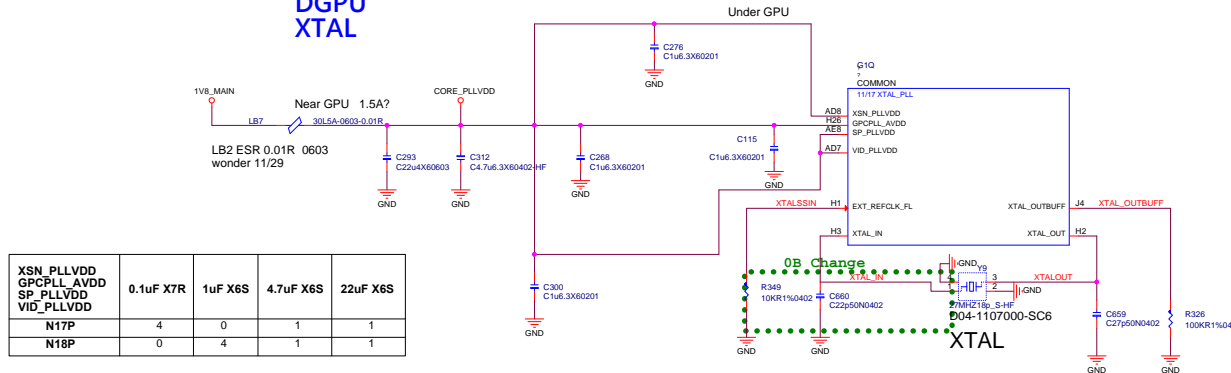


FBVDDQ	1uF X7R	10uF X6S	22uF X6S
N17P	12	6	5
N18P	12	6	5

# DACA,Display IF,XTAL



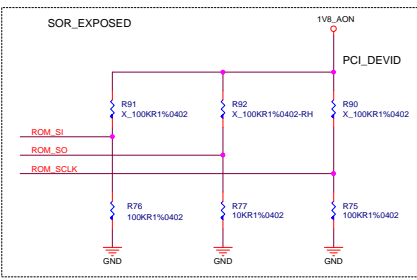
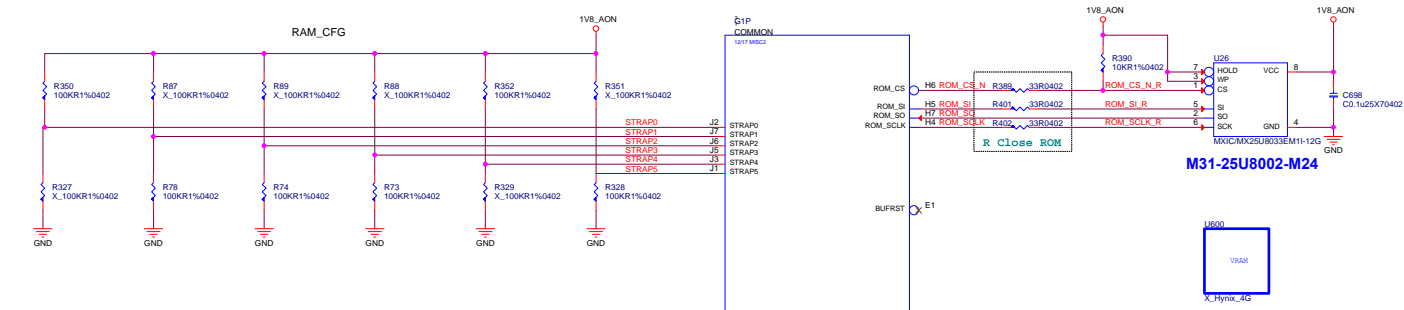
## DGPU XTAL



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Reference 14B2

# ROM, MULTI-LEVEL STRAPS



GPU	ROM_SO
N17P	100k
N18P	10k

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE FS_OVERT
H	H	M	0000	V

N17P	STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	STRAP Set
	L	L	L	0x0 Samsung: M12-8032545-S02 / K4G80325FB-HC28	4GB R116 R120 R388
	L	L	H	0x1 Micron: MT51J256M32HF-70:A	4GB R116 R120 R398
	L	H	L	0x2 Hynix: M12-5GC8H05-H23 / H5GC8H24MJR-R0C	4GB R116 R127 R388
	L	H	H	0x3 Samsung: M12-80325R5-S02 / K4G80325FC-HC25	4GB
	H	L	L	0x4 Micron: MT51J256M32HF-80:B	4GB R129 R120 R388
	H	L	H	0x5 Hynix: M12-5GC4HG5-H23 / H5GC4H24AJR-R0C	4GB R129 R120 R398
	H	H	L	0x6 Hynix: M12-5GC4HG5-H23 / H5GC4H24AJR-R0C	2GB R129 R127 R388
	H	H	H	0x7 Samsung: M12-41325A5-S02/K4G41325FE-HC28	2GB R129 R127 R398
	L	L	M	0x8 Micron: EDW032BABG-70-F:A	2GB R116 R120 R398/R388
	L	M	L		

N18P	STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	STRAP Set
	L	L	L	0x0 Samsung: K4G80325FC-HC25 :C	4GB R116 R120 R388
	L	L	H	0x1 Micron: MT51J256M32HF-80:B	4GB R116 R120 R398
	L	H	L	0x2 Hynix: H5GC8H24AJR-R2C :A	4GB R116 R127 R388

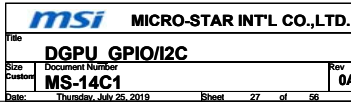
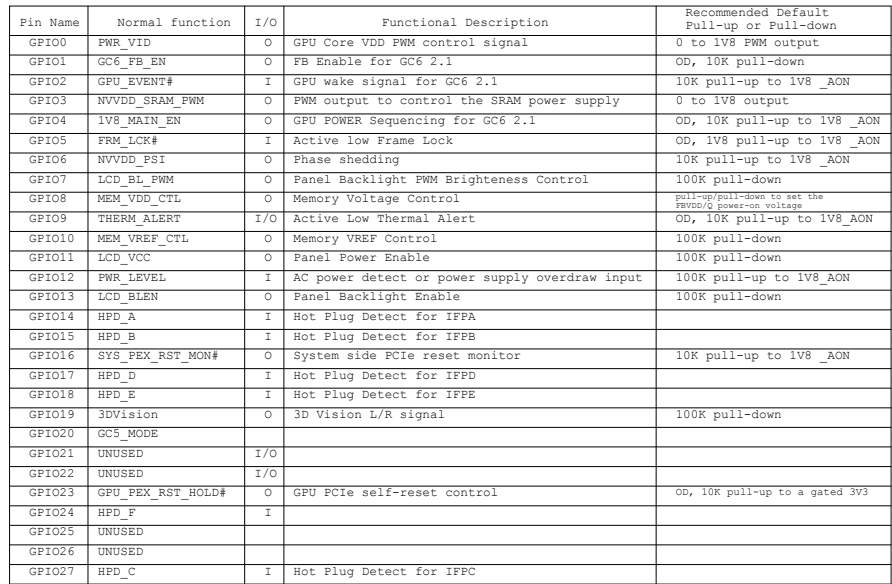
- 1:SMB\_ALT\_ADDR ENABLE
- 0:SMB\_ALT\_ADDR DISABLE
- 1:DEVID\_SEL REBRAND
- 0:DEVID\_SEL ORIGINAL
- 1:PCIE\_CFG LOW POWER
- 0:PCIE\_CFG HIGH POWER
- 1:VGA\_DEVICE ENABLE
- 0:VGA\_DEVICE DISABLE
- H=High :Tied to 1.8V
- M=Middle:Tied to 0.9V
- L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	L	0	0	0	0

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V



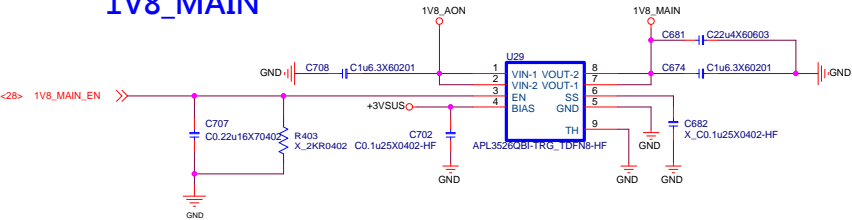


NVIDIA Power Sequence Control

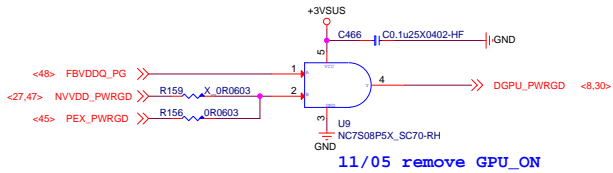
Power on = 1V8\_AON -> 1V8\_MAIN -> 3V3\_NV/NVDD -> NVDDS/PEX\_VDD -> FBVDDQ -> DGPUPWRGD

Power down = NVDDS -> PEX\_VDD -> NVVDD/FBVDDQ -> 3V3\_NV -> 1V8\_MAIN -> 1V8\_AON

1V8\_MAIN

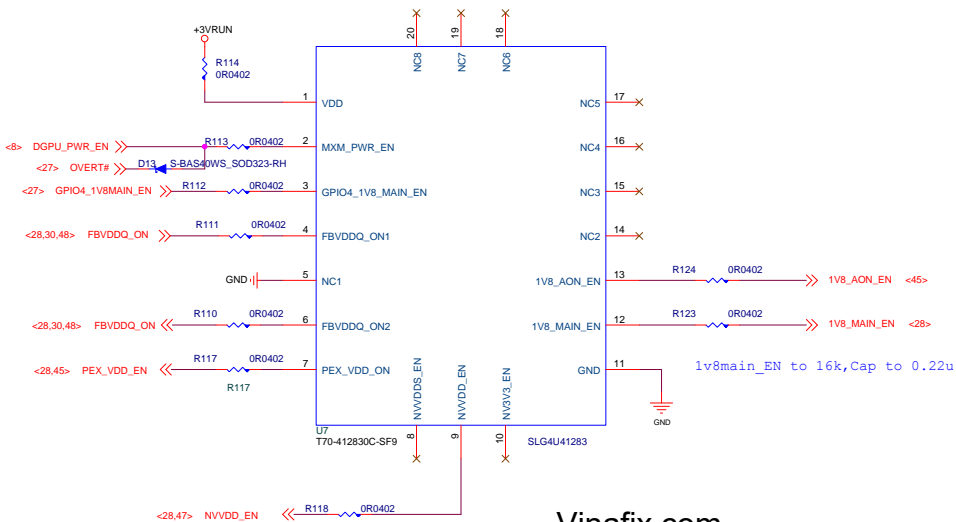


DGPU POWER GOOD



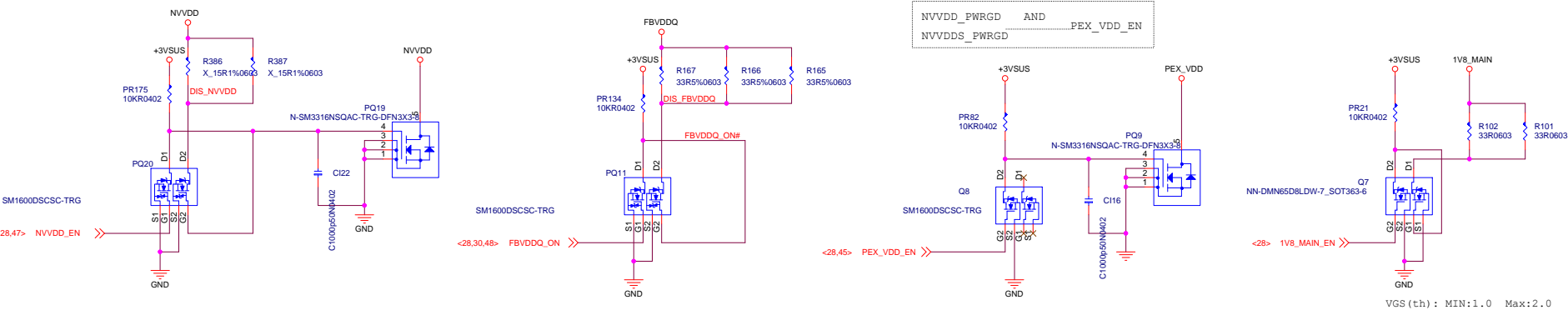
11/05 remove GPU\_ON

SLG4U41283 power sequence control IC



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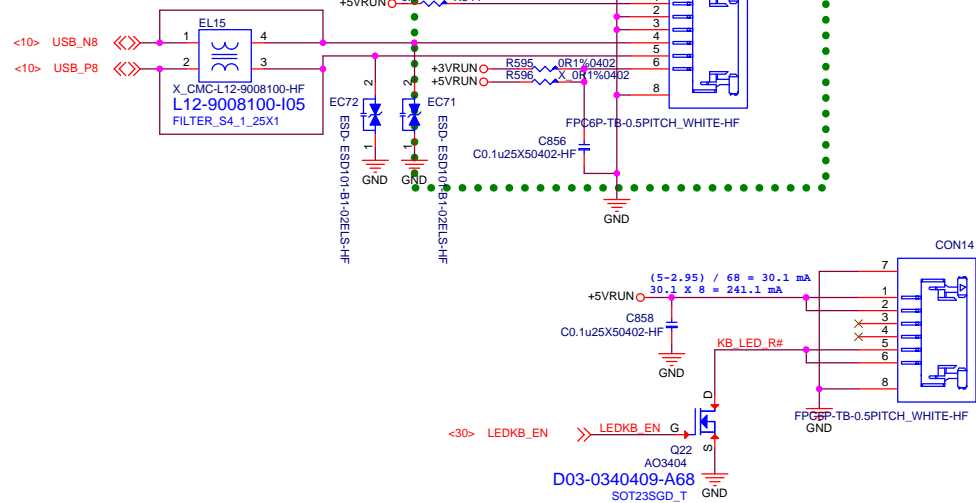
Discharge

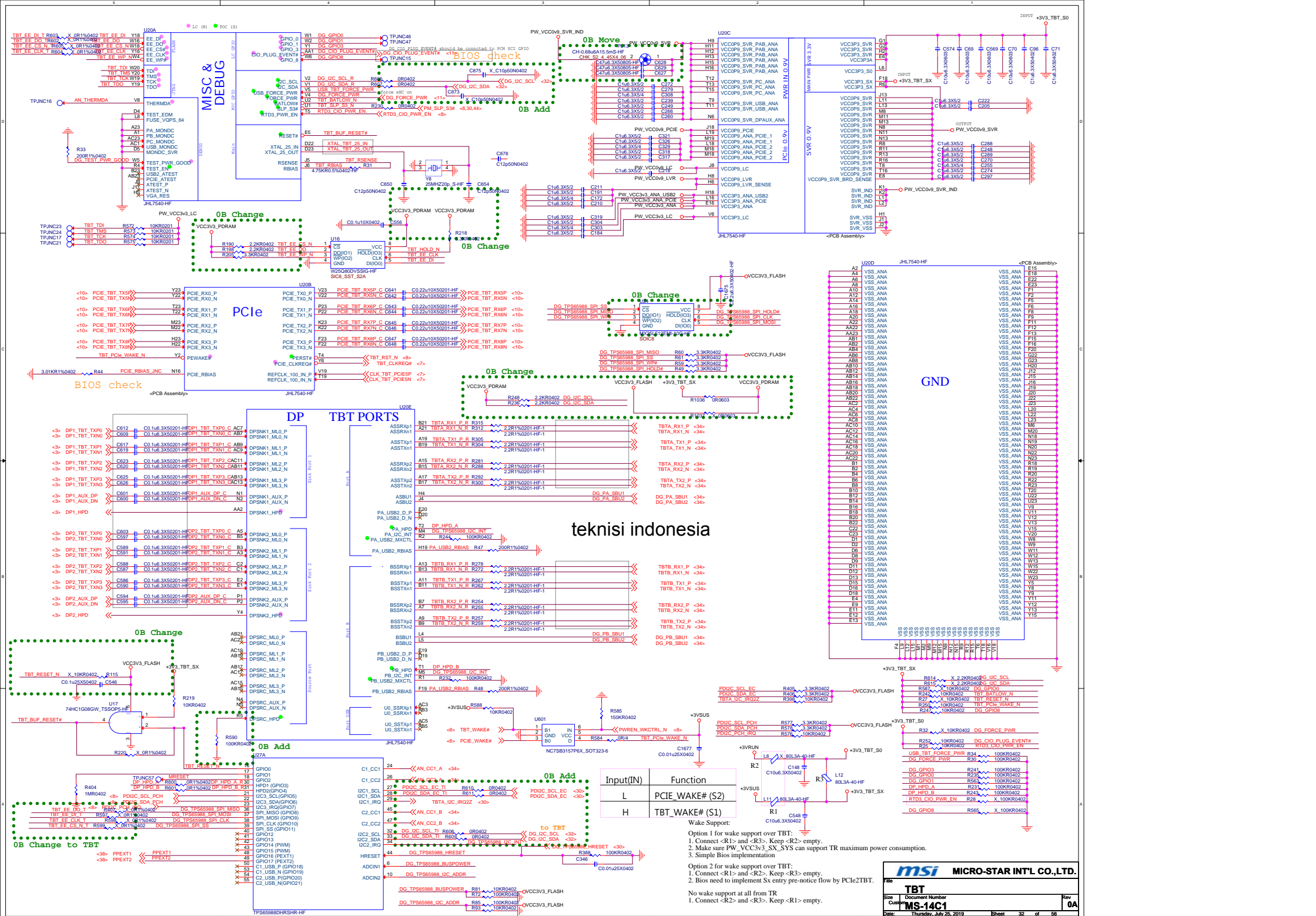




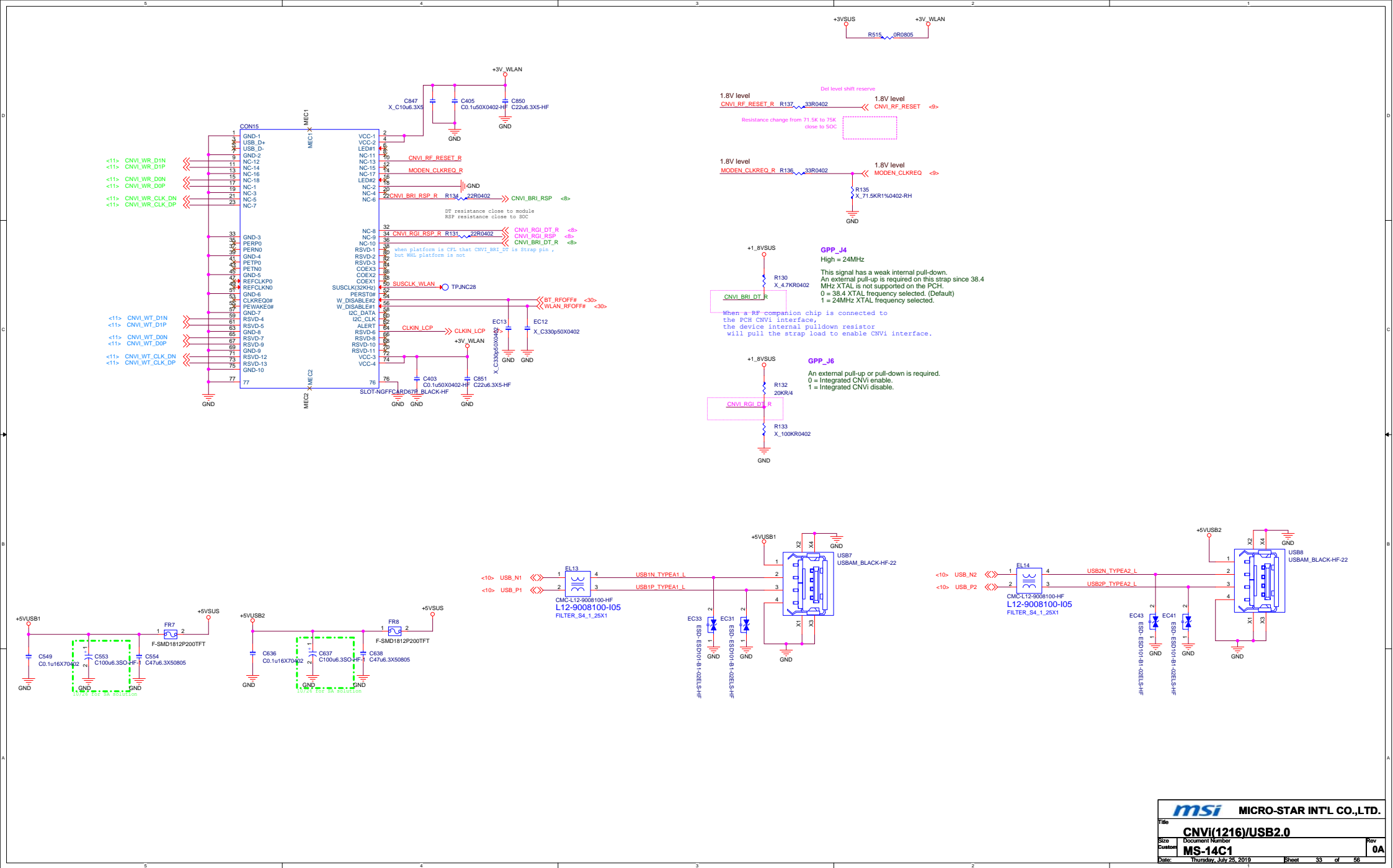


## SATA







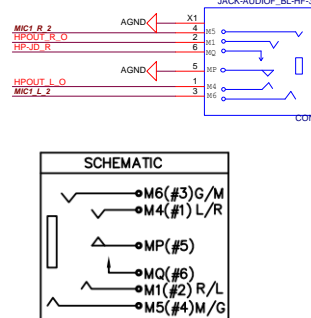
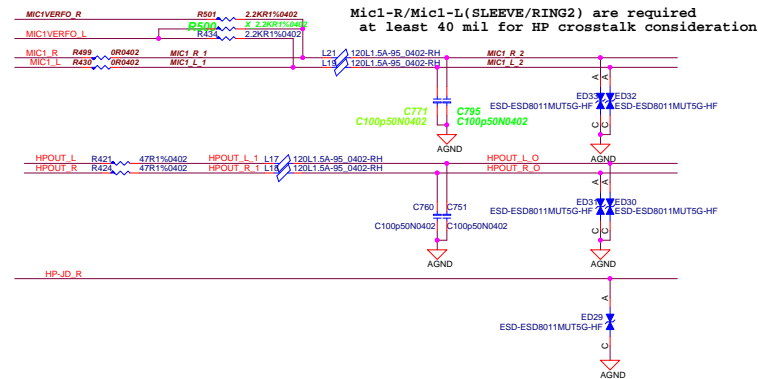


## Type C USB3.1



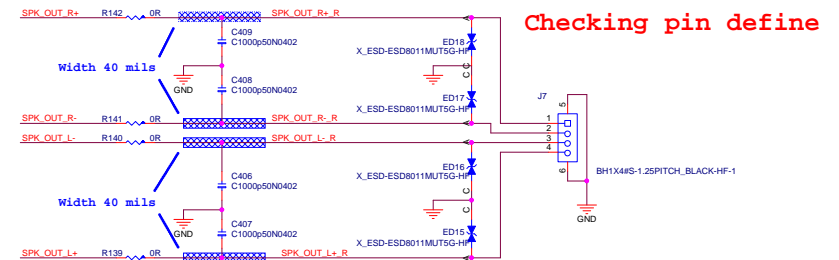
## Universal Jack

9/4 change design from Iphone type to Universal Jack



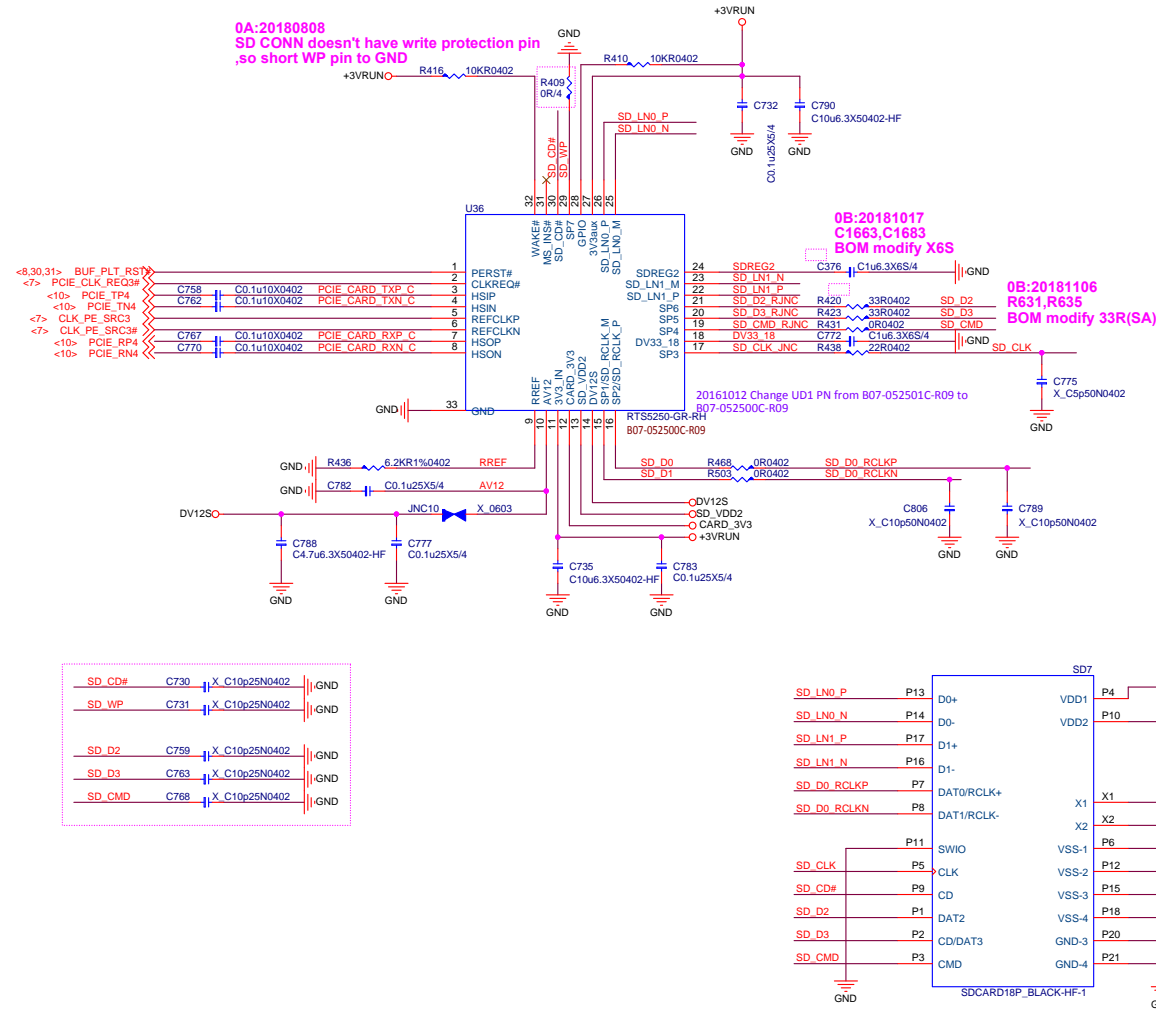
**SPEAKER**

- 1.SPK L+ L- R+ R- trace width: Speaker 4 ohm ==> 40 mils  
Speaker 8 ohm ==> 20 mils
- 2.If you mount the LC filter((L1+L4,C4/C11,C2/C7/C10/C13).Please let them together and close to codec.
- 3.Please make the trace length/ Speaker wire length of SPKL+/L-/R+/R- be the same as possible as you can.
- 4.If L1,L2,L3,L4 are replaced by 0 ohm/1.6A resistor(please don't use general bead, because it may influence the THD+N quality), and C4,C11 should be NC

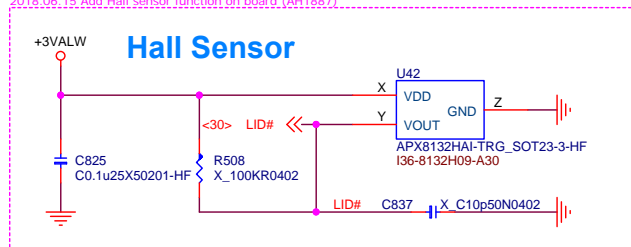


## Checking pin define

# CardReader ( RTS5250 )



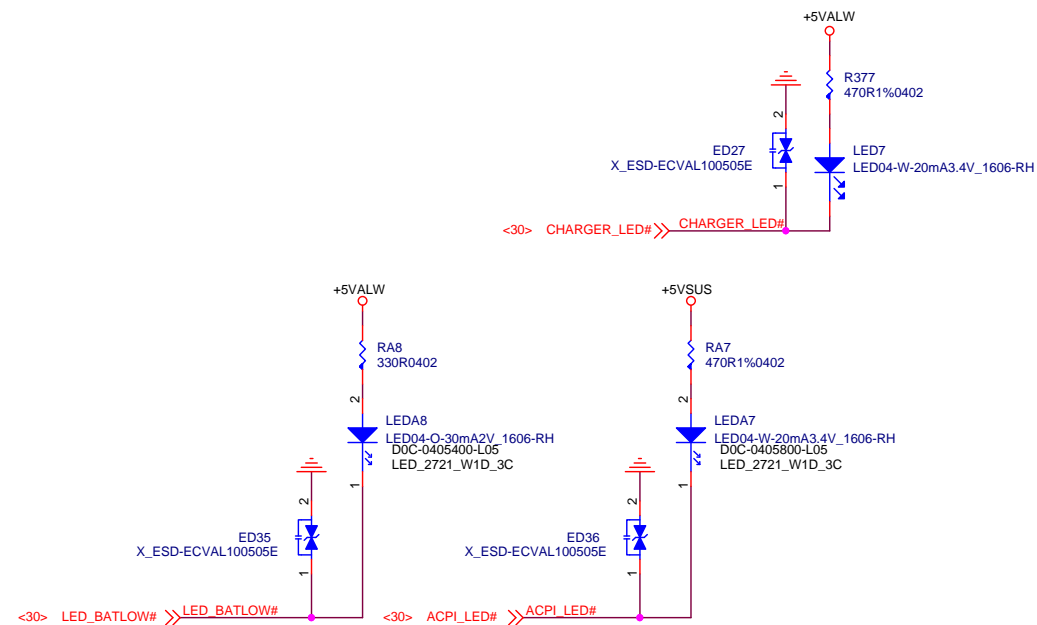
2018.06.20 Change hall sensor IC from AH1887 (2 output) to AH1810 (1 output)  
2018.06.15 Add Hall sensor function on board (AH1887)



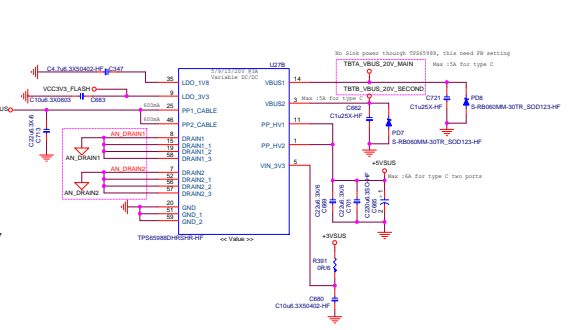
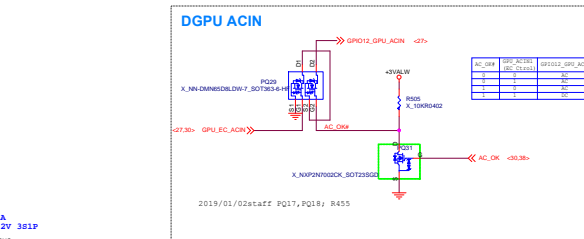
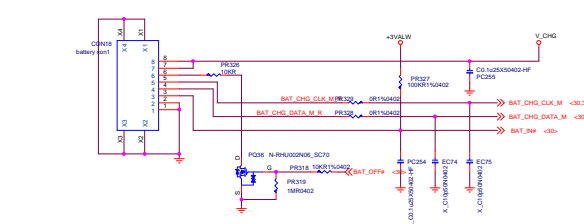
2018.06.26 Change hall sensor IC from AH1810 to APX8132 by ME suggest

## LED

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msi MICRO-STAR INT'L CO.,LTD.			
Title			
PWR SW/FP/LED/LID			
Size	Document Number		Rev
Custom	MS-14C1		0A
Date:	Thursday, July 25, 2019		Sheet 37 of 56

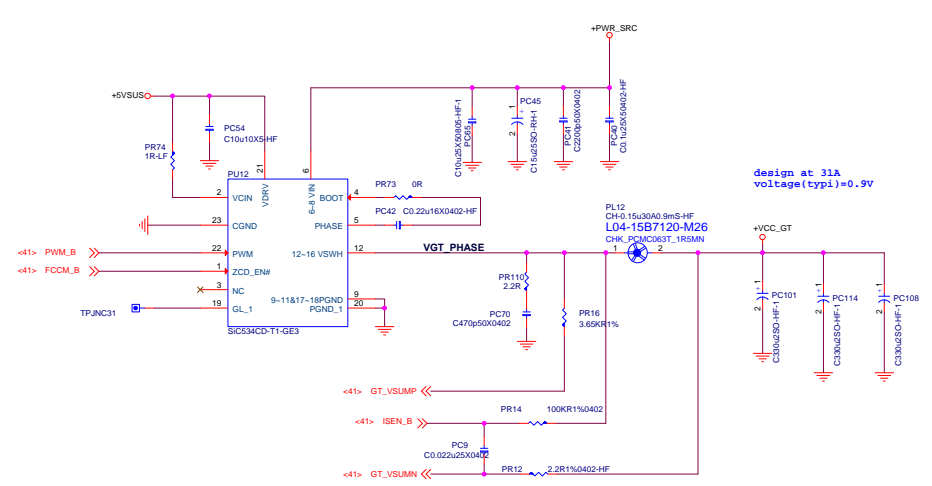
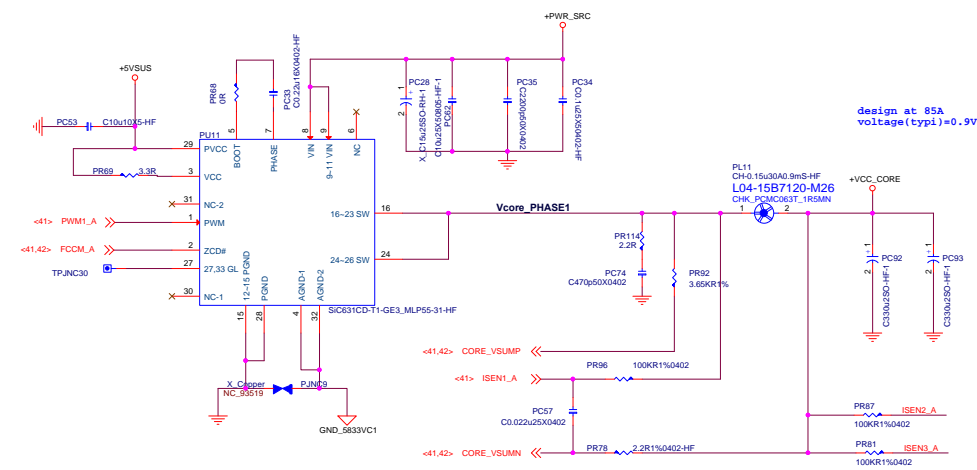
[illegible][illegible]



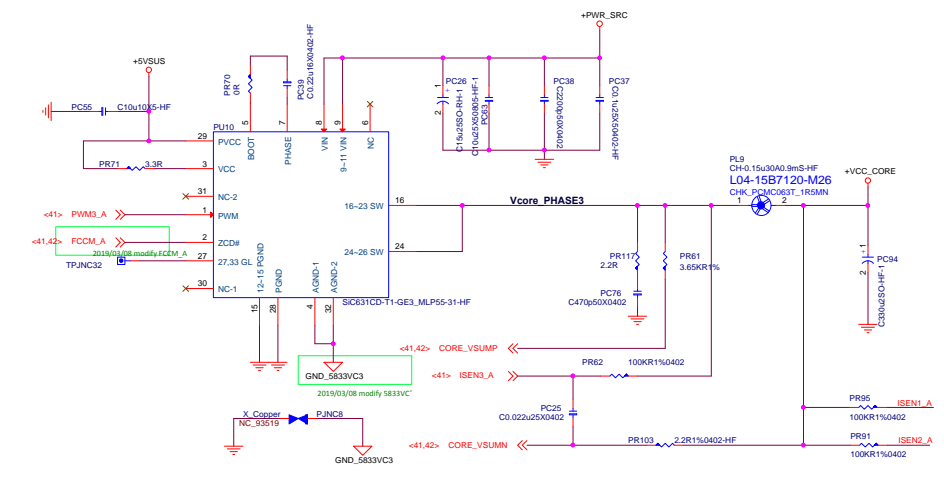
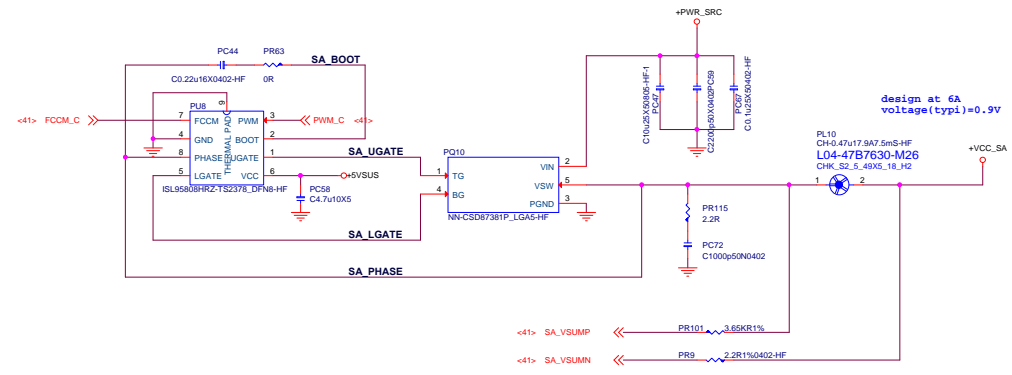
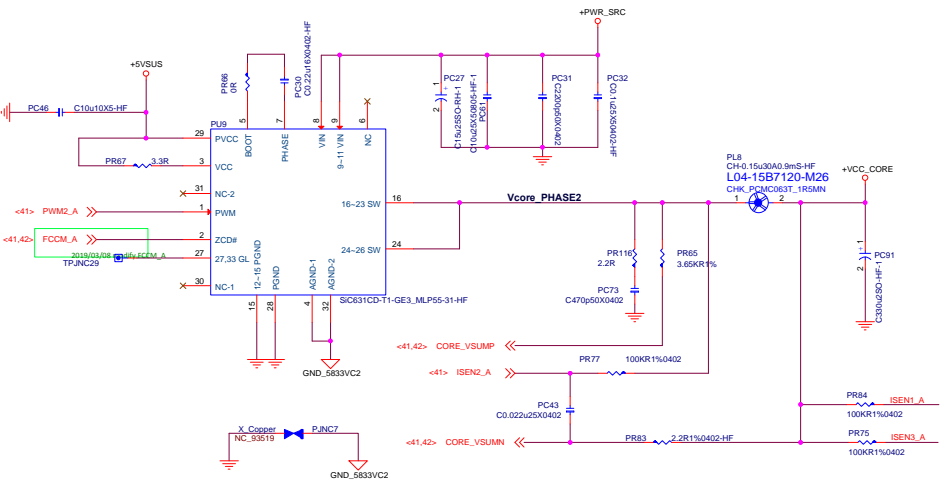








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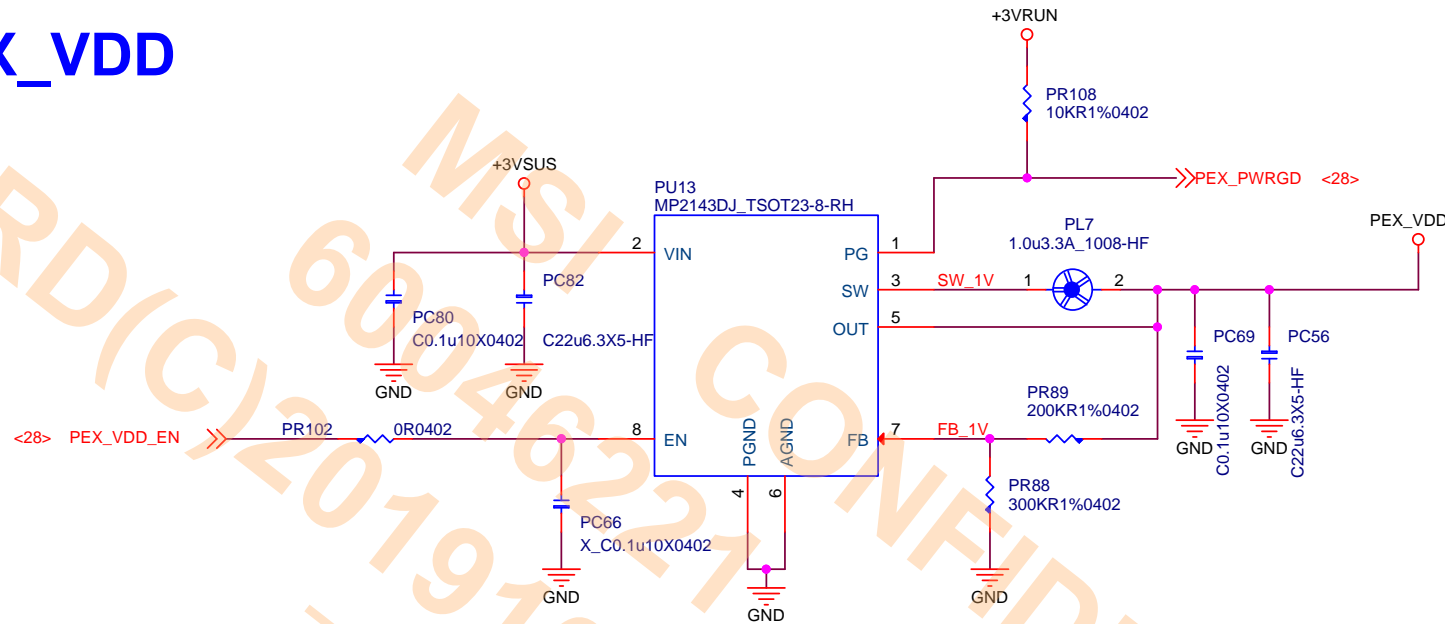




# PEX\_VDD

## PEX\_VDD

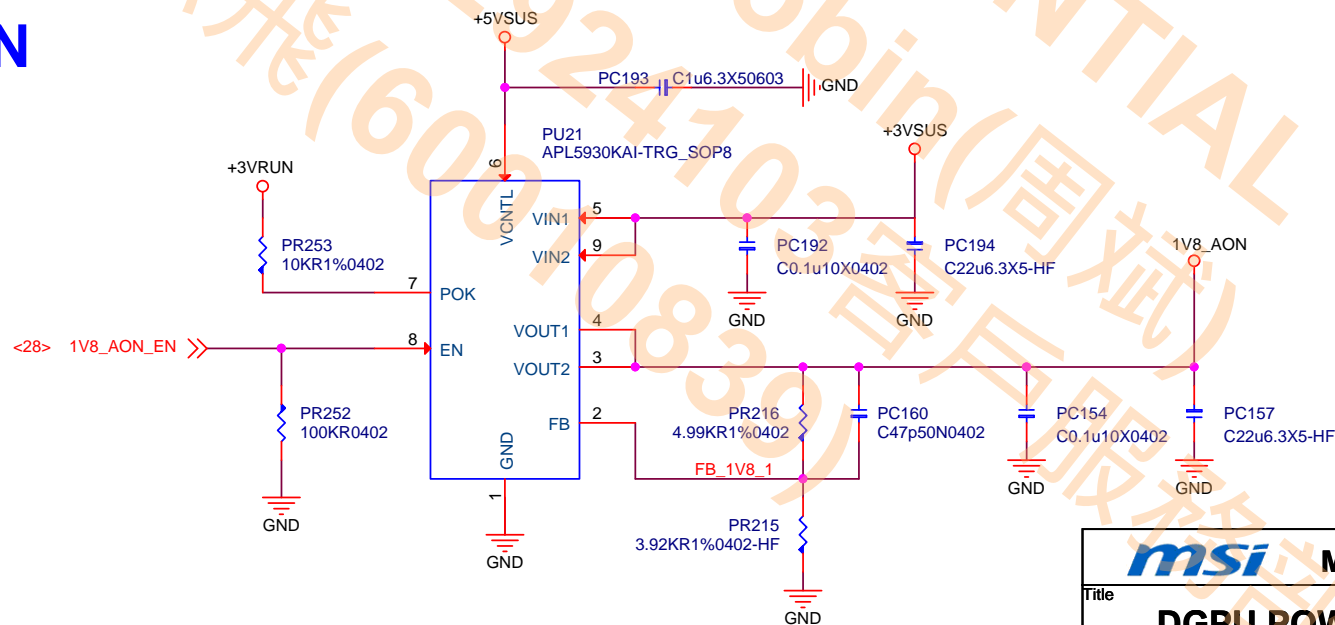
Voltage = 1.0V  
Current = 1.6A  
OCP(typi) = 4.8A



# 1V8\_AON

## 1V8\_AON

Voltage = 1.8V  
Current = 2.3A



**msi**

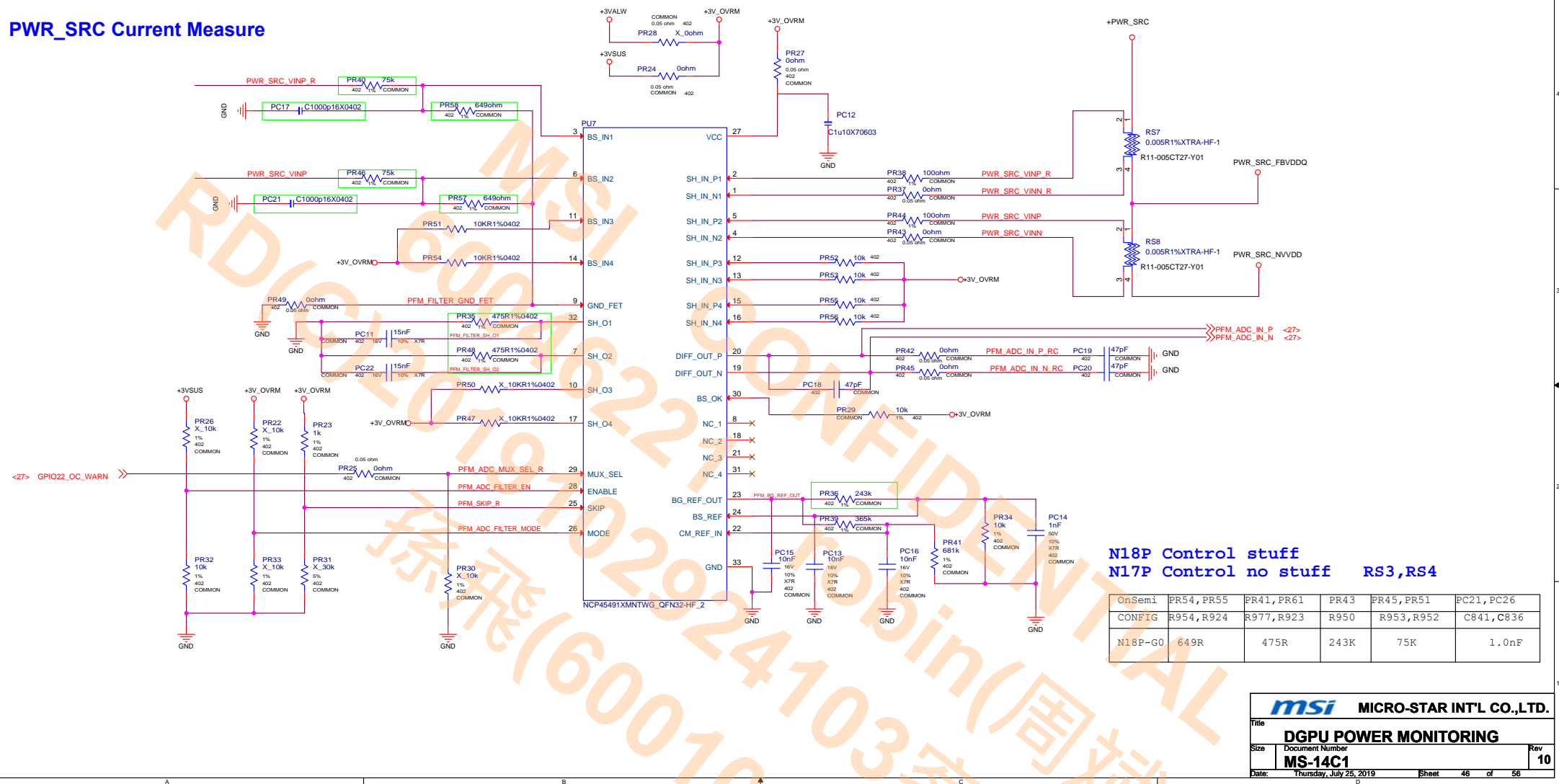
MICRO-STAR INT'L CO.,LTD.

Title  
**DGPU POWER PEX\_VDD/1V8\_AON**

Size  
Custom  
Document Number  
**MS-14C1**  
Rev  
**0A**

Date: Thursday, July 25, 2019 Sheet 45 of 56

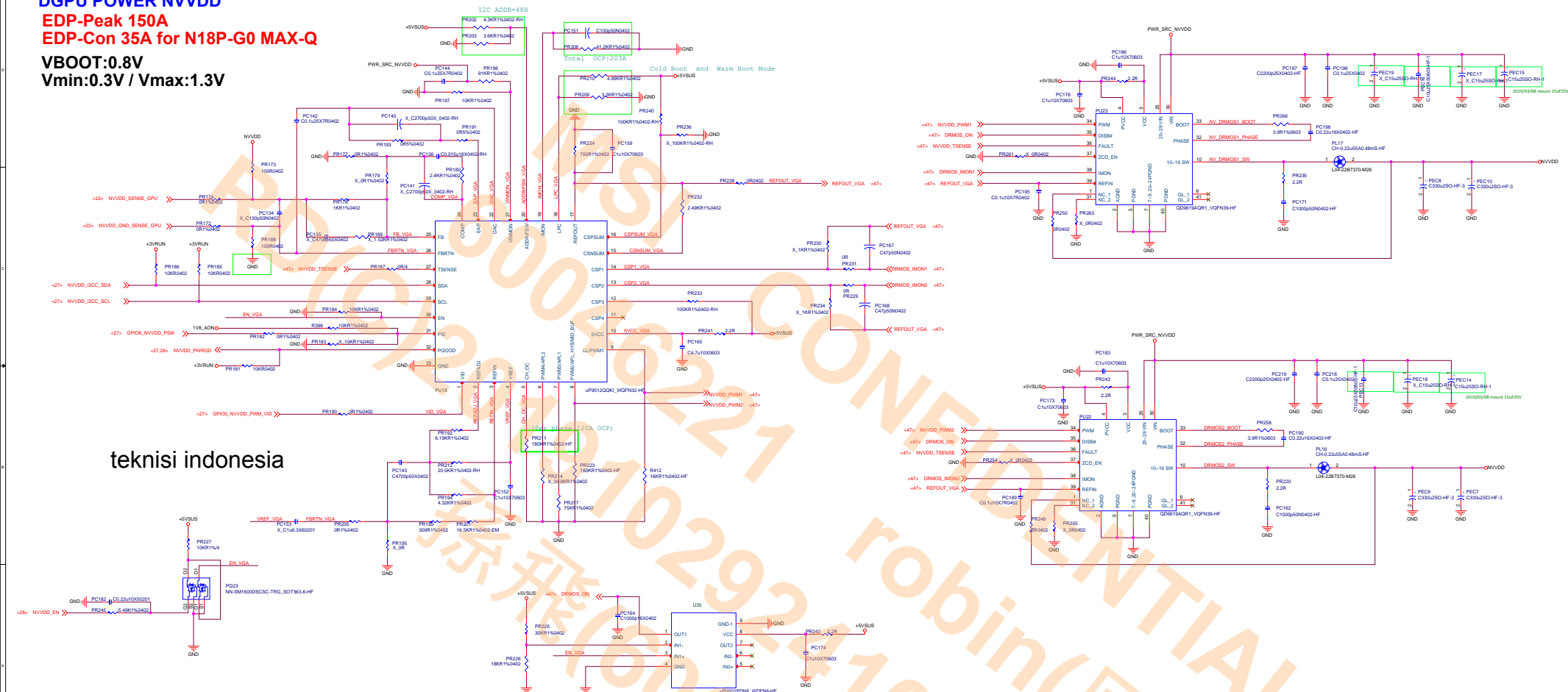
# PWR\_SRC Current Measure





**EDP-Peak 150A**  
**EDP-Con 35A for N18P-G0 MAX-Q**

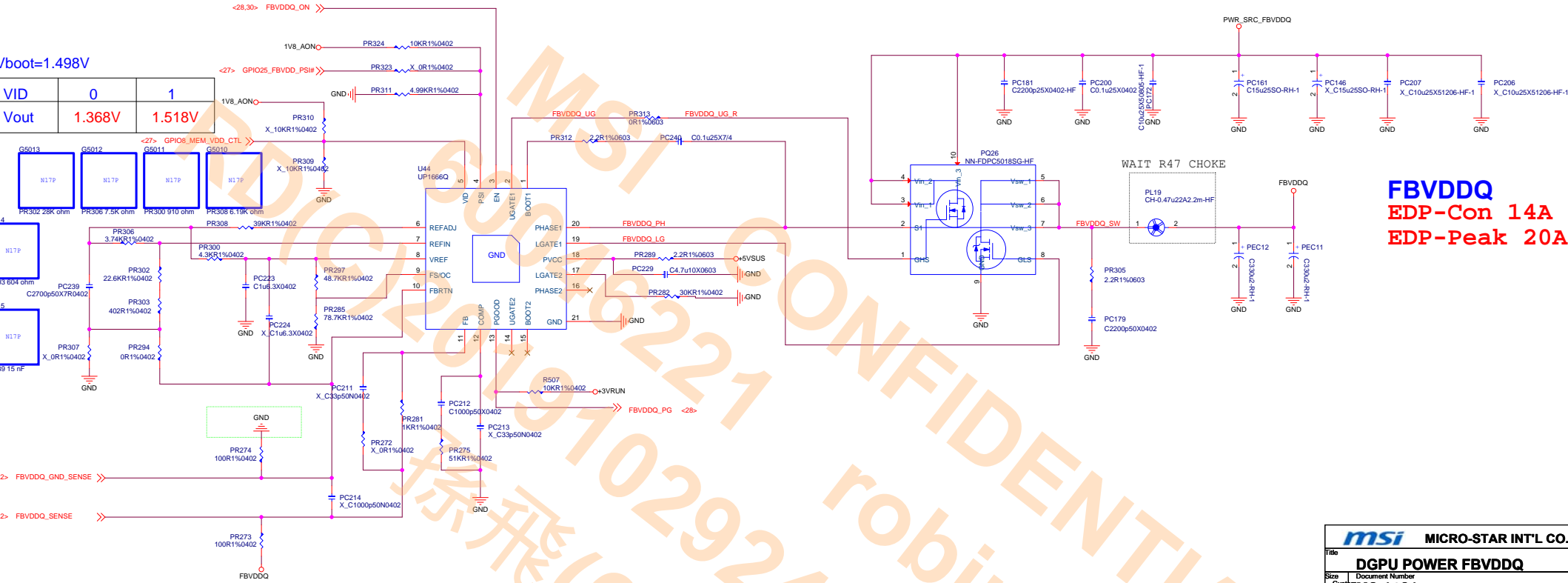
teknisi indonesia



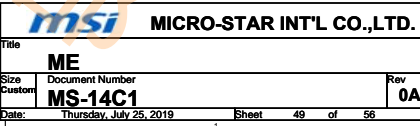
FBVDDQ

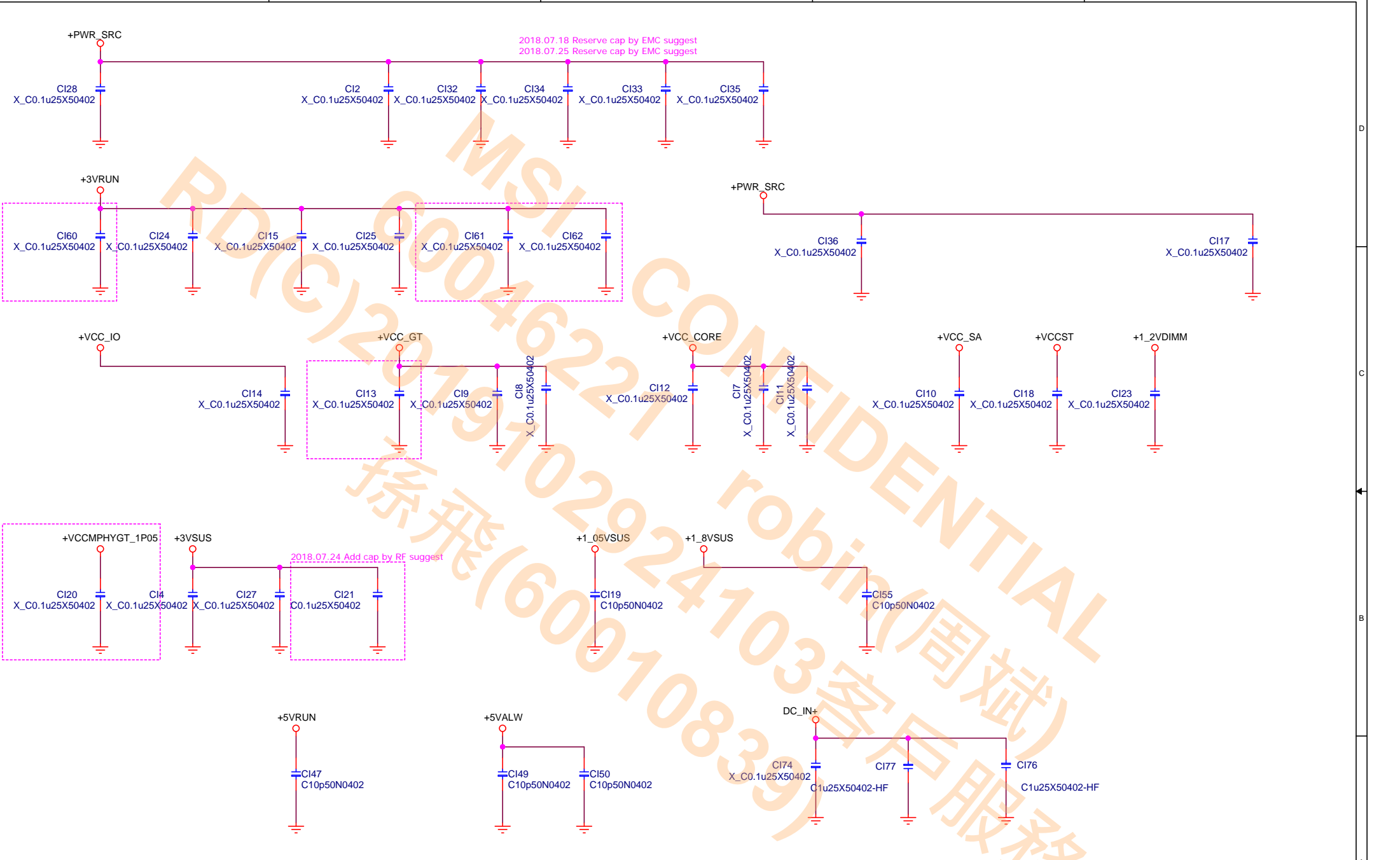
Vboot=1.498V

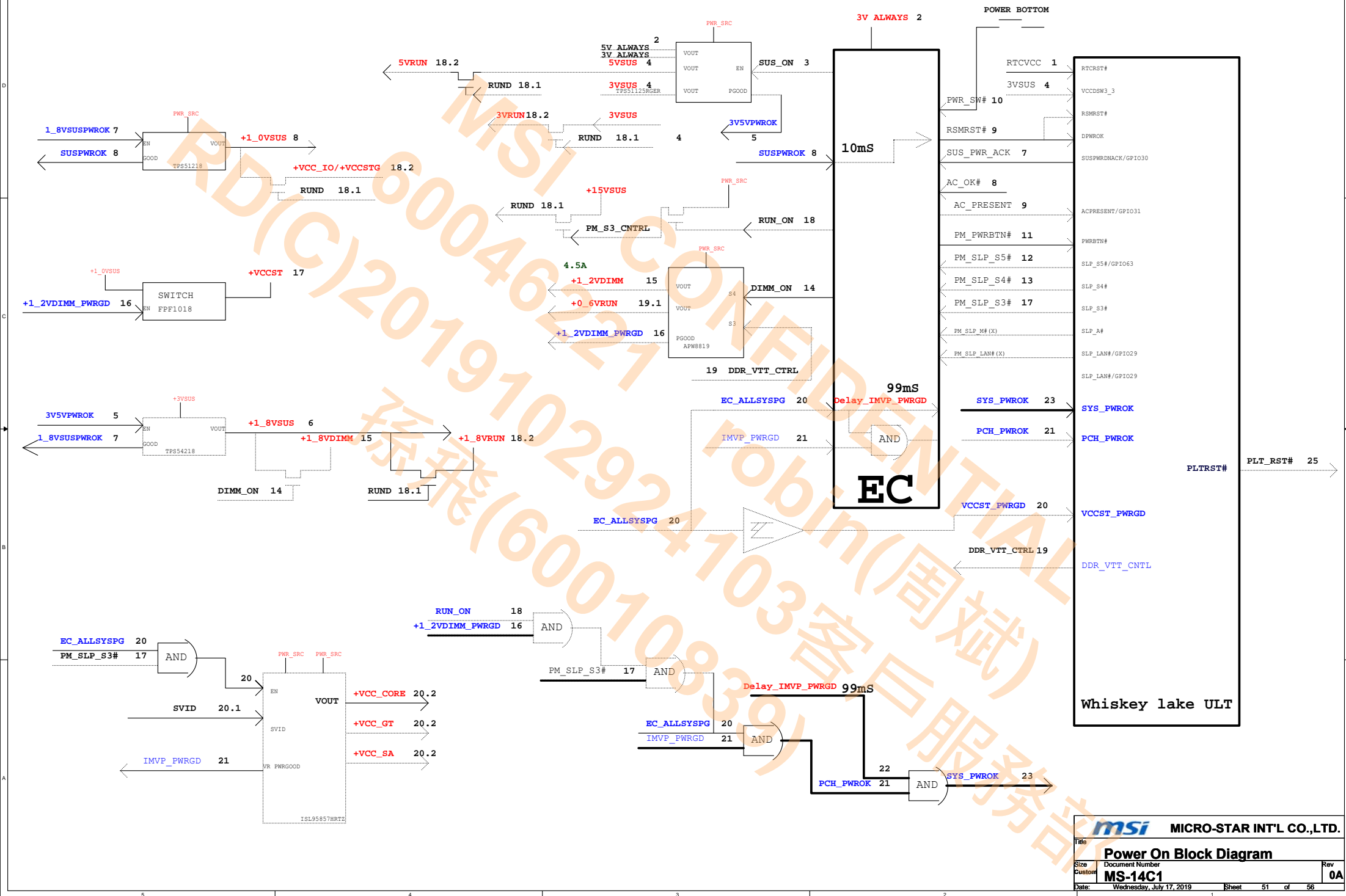
VID	0	1
Vout	1.368V	1.518V



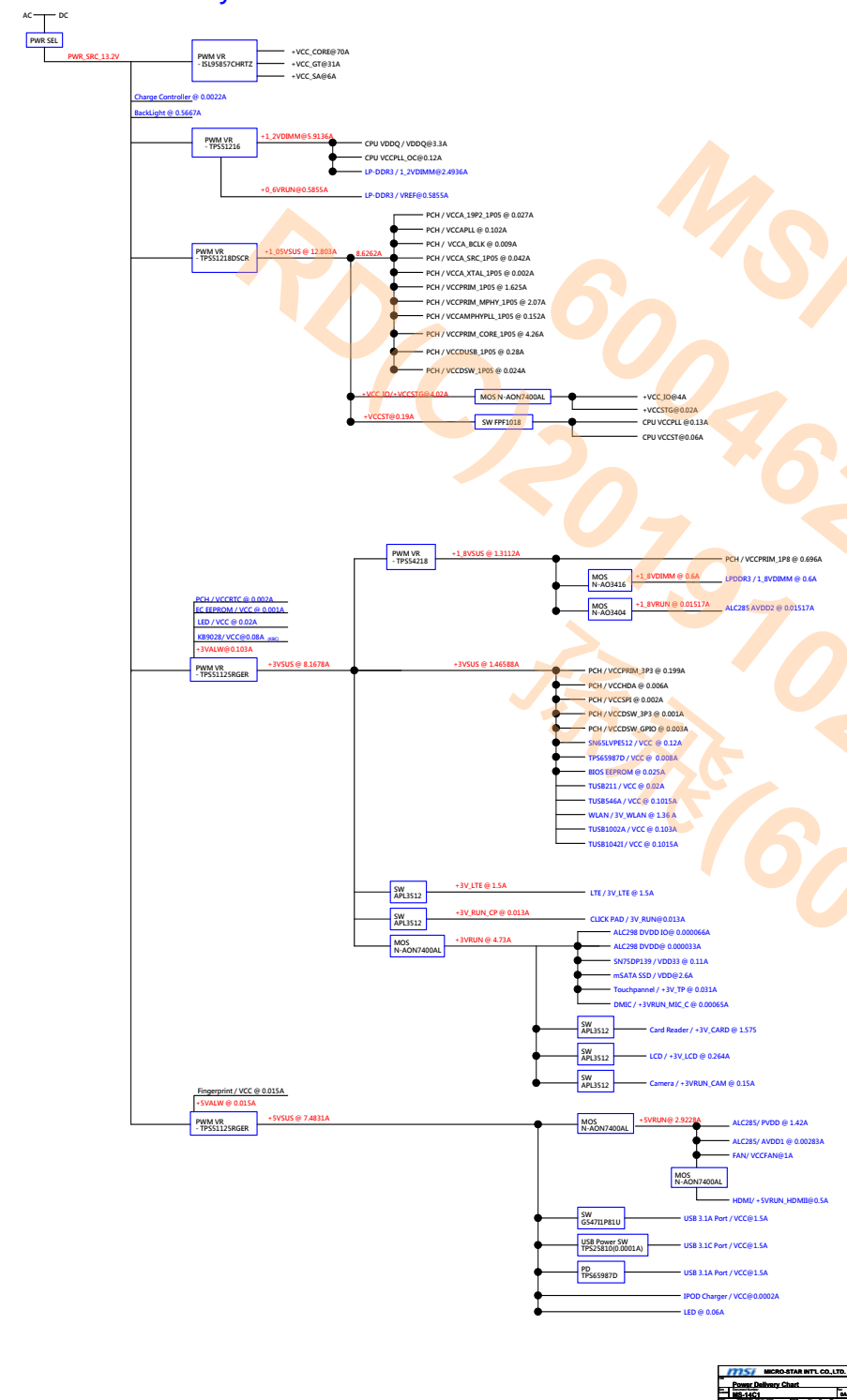
**FBVDDQ**  
EDP-Con 14A  
EDP-Peak 20A



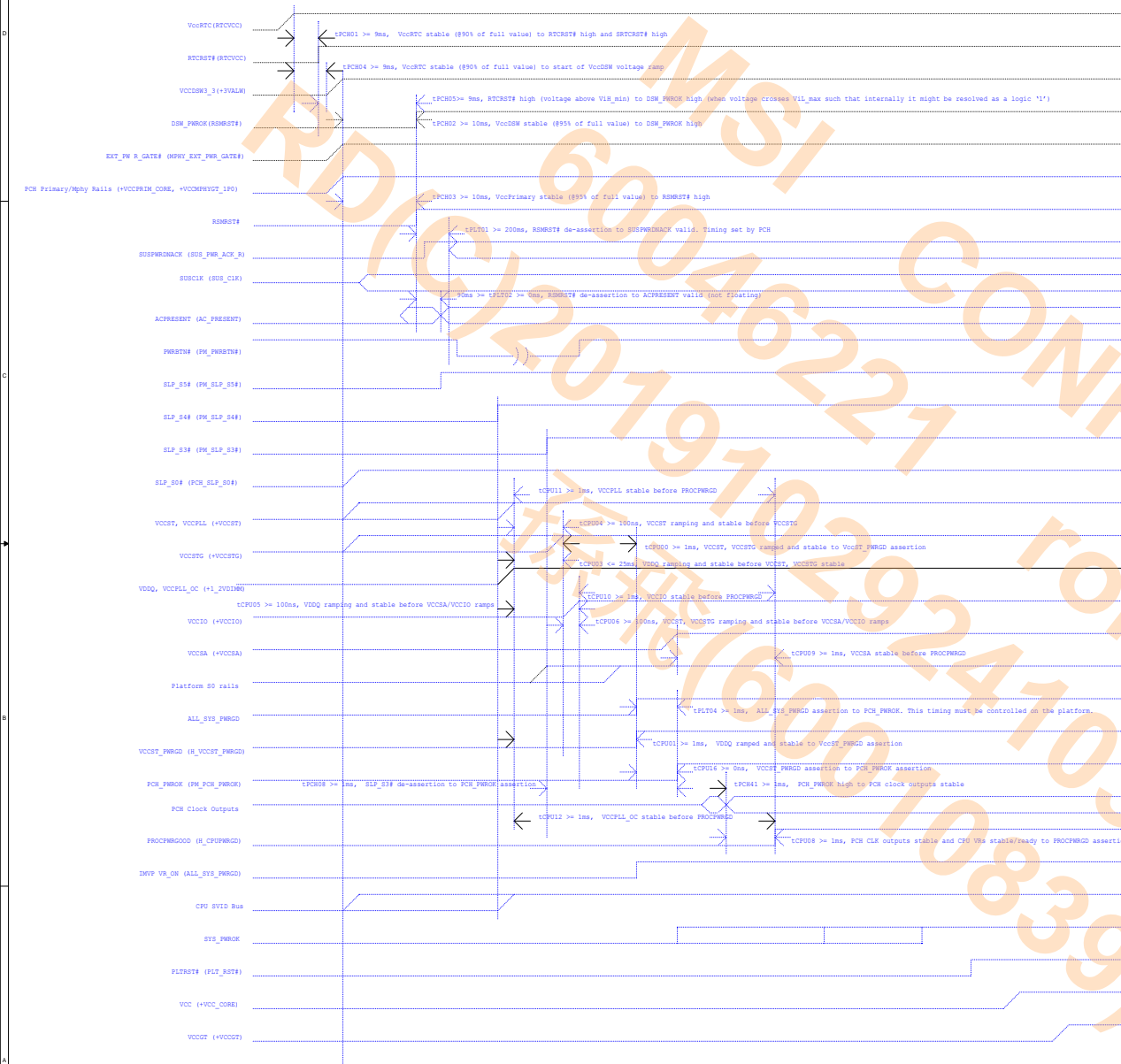




## 13H1 Power Delivery Chart



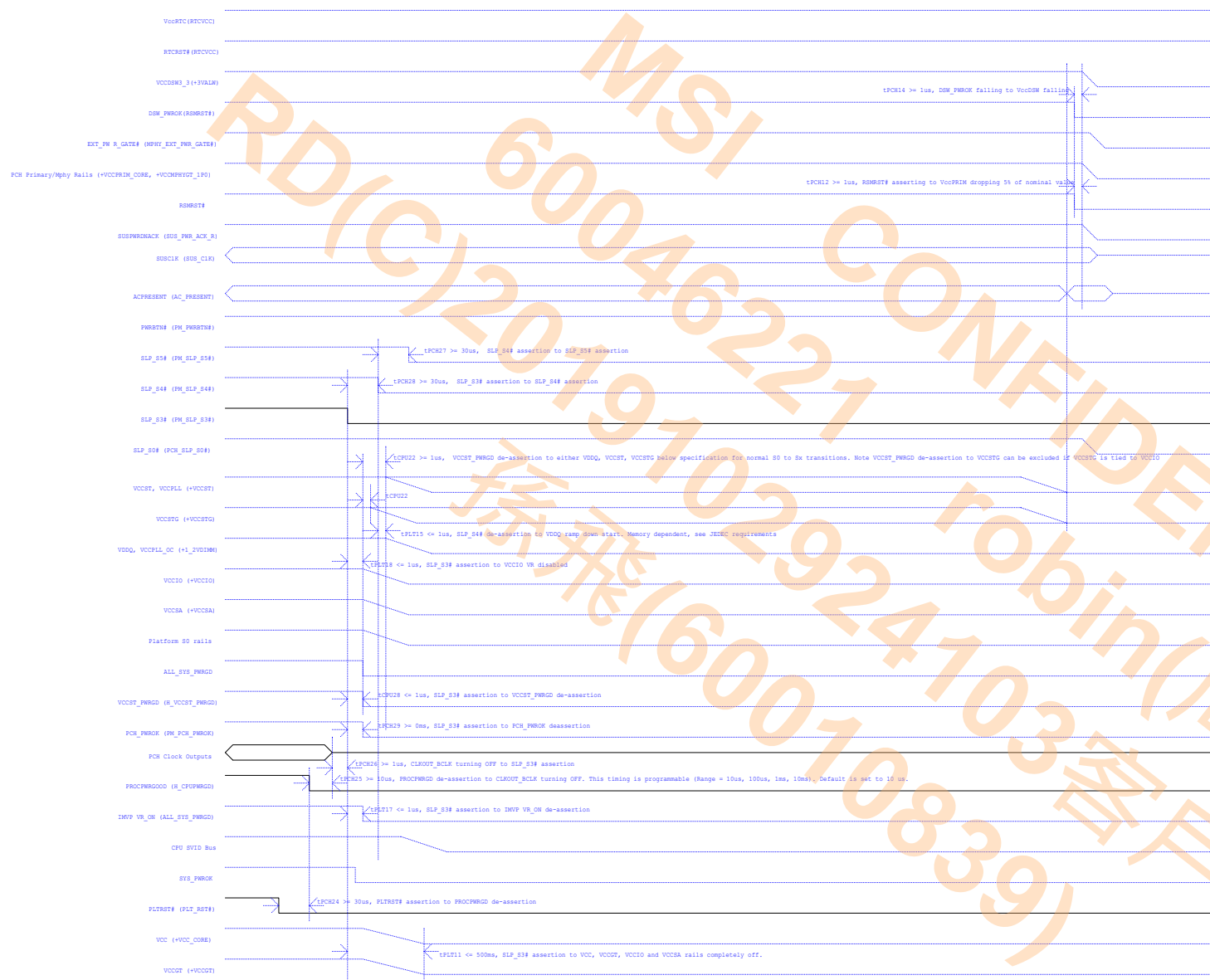
# G3 to S0



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# S0 to G3



- 497: 2018/11/02 Page18 Add R485 for TP525810 overcurrent heat issue  
498: 2018/11/02 Page18 Add Type-C\_OCR at signal for TP525810 overcurrent heat issue (Shut TP5NC173)  
499: 2018/11/02 Page11 Change signal from USB\_OC# to Type-C\_OC# for TP525810 overcurrent heat issue  
500: 2018/11/06 Page18 Update PCB shielding symbol by manufacturer suggest  
501: 2018/11/06 Page11 Un-stuff R213 because IC control pin is push-out by NEC request  
502: 2018/11/13 Page18 Change C261 from 220uf to 470uf for SA request  
503: 2018/11/13 Page11 Change R313 R314 from 0 ohm to 100 ohm by NEC request  
504: 2018/11/16 Page22 Change F2011 F2012 from AC20802 to AC20806 for USB3.0 bus break by NEC request  
505: 2018/11/16 Page25 Det F2014 F2016 and add ED109 ED110 ED111 ED112 From ES08040 to F208015M for PS-component add by NEC request  
506: 2018/11/16 Page18 Change R433 from 100 ohm to 500 ohm by NEC request  
507: 2018/11/16 Page25 Change R422 from 243 ohm to 390 ohm by NEC request  
508: 2018/11/19 Page20 Remove L1M633 by ME request  
509: 2018/11/19 Page24 Change R17 value from 2.2kOhm to 10kOhm for ME cannot be detected  
510: 2018/11/22 Page18 Det RTC crystal 2nd source, Remove RTC crystal virtual component(976)  
511: 2018/11/22 Page18 Add virtual component for JSM crystal by different ROM(977)  
512: 2018/11/22 Page17 Shift EC115,EC116,EC18,EC19 by EM suggest  
513: 2018/11/27 Page27 Change C418 from 100uf to 220uf for voltage drop of +5V\_LTE  
514: 2018/11/29 Page18 Change ME voltage(L1M630) main source from EDP-3W12012-1.5W0 to EDP-3W12012-1.5W2 by ME request  
515: 2018/11/29 Page24 Change T10A1002A setting for vendor suggest(CH2\_C402\_C02 from 1.0 to R4) Un-stuff R215, Un-stuff R216 Change R213 from 1K ohm to 20K ohm  
516: 2018/11/29 Page18 Add WiFi Module Mxler by ME request (L1M630)  
517: 2018/11/29 Page18 Add Power Adapter Type 2 by ME request (L1M631)  
518: 2018/11/29 Page18 Add Power Adapter Type 3 by ME request (L1M632)  
519: 2018/11/29 Page18 Add Router (Square) by ME request (L1M633)  
520: 2018/11/29 Page18 Add Router (Square) by ME request (L1M634)  
521: 2018/11/29 Page18 Add Router (Circle) by ME request (L1M635)  
522: 2018/11/29 Page18 Add SMA Connector Mxler by ME request (L1M636)  
523: 2018/11/29 Page18 Change PCB 976 from PDS-13W12012-1.5W0 to PDS-13W12012-1.5W2 by ME request  
524: 2018/11/19 Page23 Un-stuff R215 for Type-C USB3.1 GEN2 compliance test by NEC request  
525: 2018/11/16 Page23 Change R215 R123 from 20K ohm to 1K ohm for Type-A compliance test by NEC request  
526: 2018/11/17 Page18 L1M670 and L1M671 change to Un-stuff by ME request  
527: 2018/12/17 Page18 Add Thermal UDR Sponge for S063 by ME request (L1M672)

